

Nonoverlapping Power/Ground Planes for Suppression of Power Plane Noise

Arif Ege Engin¹, *Member, IEEE*, Ivan Ndip, *Senior Member, IEEE*, Klaus-Dieter Lang, *Senior Member, IEEE*, and Gerardo Aguirre, *Senior Member, IEEE*

Abstract—Providing low *IR*-drop and inductance are two major roles of power and ground (PG) planes in chip packages and boards. However, planes can also cause switching noise coupling, especially when they resonate. This is a concern for mixed-signal boards, high-speed I/Os, and electromagnetic compatibility. Discrete decoupling capacitors are ineffective to control switching noise at gigahertz frequency regime due to their inductance. To filter such high-frequency noise, a possible approach is modifying the shape of the PG planes, such as in power islands or electromagnetic bandgap structures. In this paper, we introduce the nonoverlapping PG planes design methodology for filtering of gigahertz power plane noise. Unlike existing approaches, our approach is simple and has wide bandwidth, while avoiding narrow inductive bridges that increase *IR*-drop.

Index Terms—Materials characterization, power and ground (PG) planes, power distribution network, power integrity, simultaneous switching noise.

I. INTRODUCTION

CHIP packages and printed circuit boards make use of power/ground (PG) planes to improve power integrity in two main aspects. They provide a low resistance (i.e., low *IR*-drop) connection from the chip terminals to the power supply. To control *IR*-drop, multiple PG layers in a stack-up with thick metals can be used. At higher frequencies, the same PG planes can also provide a low inductance connection to the off-chip decoupling capacitors if PG layers are stacked in an alternating manner. On many package and board stack-ups, it is, therefore, a common practice to allocate several layers in an alternating manner to PG planes.

Low *IR*-drop and low inductance properties of PG planes do not, however, necessarily provide low impedance at higher frequencies. PG planes cause undesirable antiresonances, as they interact with the decoupling capacitors or when their sizes exceed half a wavelength. This high impedance is especially

a concern for mixed-signal boards, high-speed I/Os, and electromagnetic compatibility. In a mixed-signal board, the sensitive analog/RF circuits may require high levels of isolation from switching noise. High-speed I/Os may experience crosstalk noise coupled globally through the PG planes. Finally, edge radiation from PG planes is one of the main sources for electromagnetic interference. The coupling of switching noise in these cases depends on the transfer impedance of the power distribution network.

Traditional solution to control switching noise is based on decoupling capacitors, which, however, become ineffective due to their inductance in gigahertz frequency regime. Therefore, special patterned power planes, such as power islands/archipelago [1], [2] or electromagnetic bandgap structures [3]–[6], have been used to reduce the transfer impedance. These designs provide a low-pass filter response by generating capacitive patches on the power plane connected by narrow inductive bridges. These narrow bridges, however, significantly increase the *IR*-drop of PG planes and result in signal integrity issues for I/Os that need to run over slits in the power plane. Another approach is based on using quarter-wave resonators as a distributed substitute for discrete decoupling capacitors. At the design frequency, the resonators create an ac short circuit between the PG planes. An array of such resonators then can be placed in electrically short intervals to create a virtual ground fence [7]–[10]. This bandstop-type filter is mostly suitable for narrowband systems due to the nature of quarter-wave resonators.

In this paper, we discuss the nonoverlapping PG (no-PG) planes design methodology for filtering of gigahertz power plane noise. This approach directly controls the coupling of switching noise globally on a package or board. The design procedure is simple and results in broadband isolation. It is based on using traditional alternating PG layers for designing locally the power distribution network of each IC on a board. The local power distribution networks are connected with each other using no-PG planes that provide ultimate noise isolation. The presented no-PG planes design methodology for the first time provides broadband filtering of power plane noise while avoiding narrow inductive bridges that increase *IR*-drop. The basic design approach for no-PG planes has been introduced in [11]. In this paper, we present design options for the no-PG planes depending on the board size, port location, segment separation, and segment size.

II. NONOVERLAPPING POWER/GROUND PLANES

A typical four-layered board stack-up is shown in Fig. 1(a). The closely spaced PG planes are desired for low inductance

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A. E. Engin is with the Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA 92182 USA (e-mail: aengin@mail.sdsu.edu).

I. Ndip is with the Department of RF and Smart Sensor Systems, Fraunhofer-Institut fuer Zuverlaessigkeit und Mikrointegration, 13355 Berlin, Germany.

K.-D. Lang is with the Fraunhofer-Institut fuer Zuverlaessigkeit und Mikrointegration, 13355 Berlin, Germany.

G. Aguirre is with Kyocera International, Inc., San Diego, CA 92111 USA. Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

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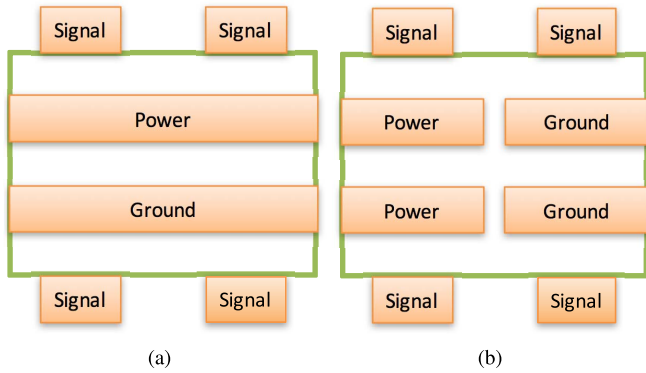


Fig. 1. (a) Traditional PG layers in a typical four-layered board. (b) no-PG layers designed as PP or GG layers.



Fig. 2. Example layout with 3×2 PG segments that would be interconnected with low IR -drop, but isolated from each other at high frequencies due to PP and GG segments.

connection of off-chip decoupling capacitors. Therefore, it is assumed that locally each IC on a multichip board will be placed on top of traditional alternating PG layers. The PG planes in this layer stack-up, however, behave as parallel-plate waveguides and allow propagation of switching noise globally across the whole board, especially at the antiresonance frequencies. To completely eliminate the parallel-plate currents, we propose to use power/power (PP) and ground/ground (GG) segments in the stack-up, as shown in Fig. 1(b). The no-PG plane segments in the form of PP or GG planes globally filter switching noise.

The PP and GG segments are used to serve as isolating elements among PG segments while preserving dc connectivity in the layout. An example layout could then look, as shown in Fig. 2, where there are 3×2 PG segments that would be interconnected with low IR -drop, but isolated from each other at high frequencies. Any small gaps, such as the two empty squares in the example layout, can then be filled with PP or GG segments. Although the example is given for a single PG plane pair, this new design approach can be extended to designs with arbitrary number of PG layers.

III. EXAMPLE DESIGN

To demonstrate the performance of no-PG planes, a two-layered board was designed, as shown in Fig. 3. The board

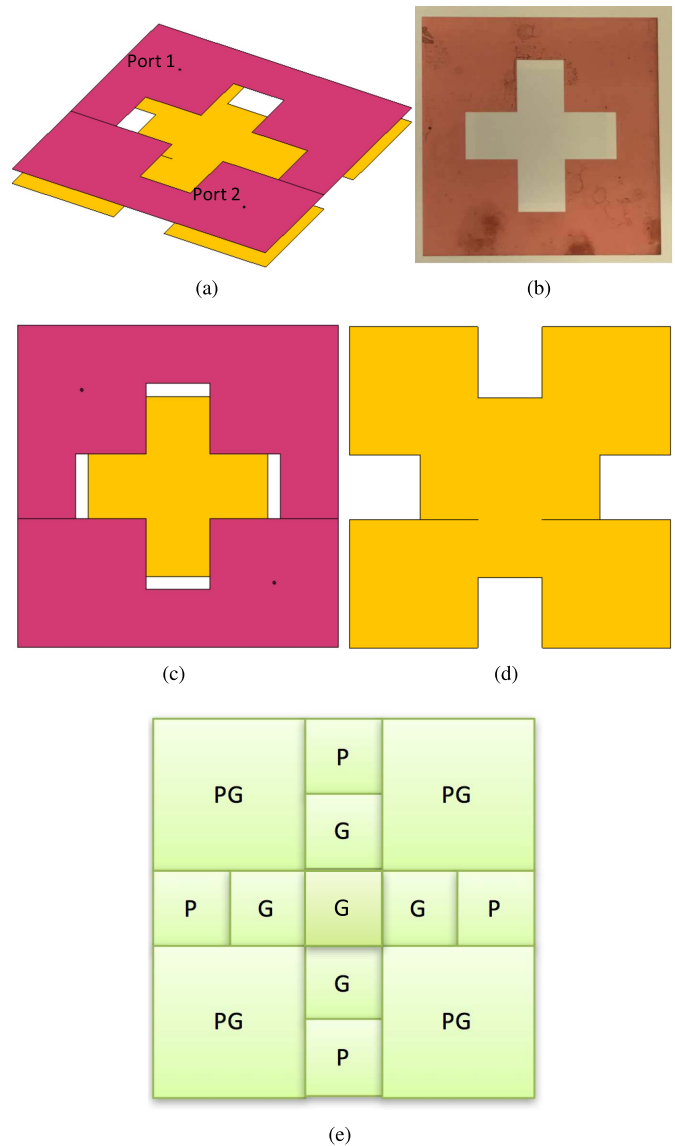


Fig. 3. LCP board with no-PG planes. (a) 3-D view. (b) Picture of the test coupon. (c) Top view. (d) Ground plane. (e) Corresponding layout segmentation with 2×2 PG segments isolated from each other at high frequencies due to P and G segments.

consists of 2×2 PG segments that are interconnected with P and G segments. In this design, P and G segments were preferred to be able to easily visualize the concept. The isolating P and G segments could be extended to PP and GG segments, respectively, using vias to maintain low IR -drop.

In a practical board design, PG planes can come in arbitrary shapes and include cutouts or via holes. For such arbitrary plane shapes, the same design principles can be applied as well, by avoiding the overlap of PG planes in isolating segments. The signal integrity of transmission lines also needs to be considered. There will be a return path discontinuity for transmission lines running over cut regions. However, this problem is not as severe as in electromagnetic bandgap structures or power islands that require narrow bridges. The wide P and G segments can allow a continuous wide return path for transmission lines running across isolated segments.

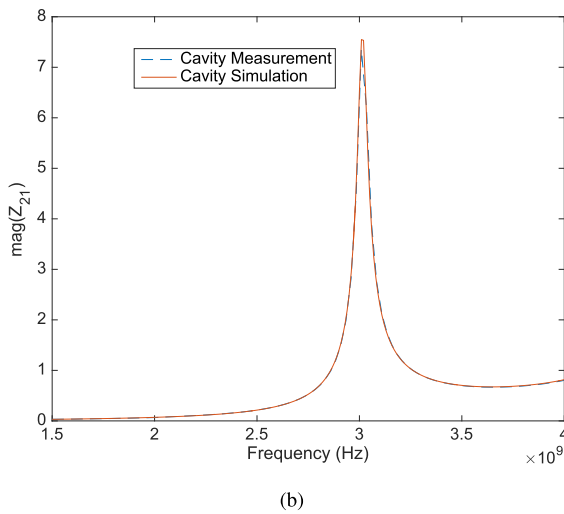
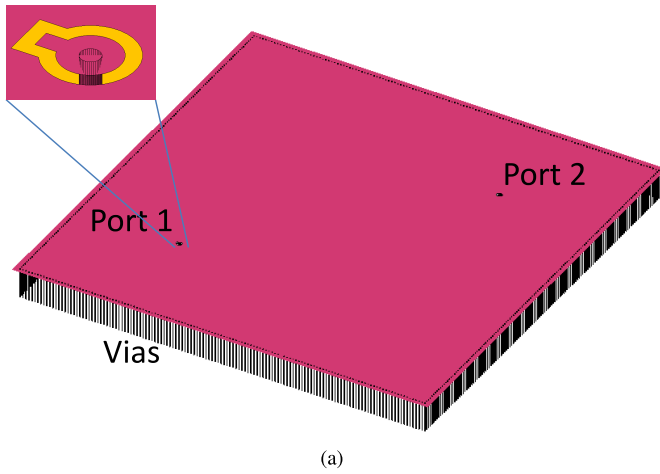


Fig. 4. (a) Cavity resonator of size 4.05 cm \times 4.05 cm to extract the dielectric thickness (DT), constant (DK), and loss tangent (DF). The inset shows the zoomed-in-view area around the measurement port. (b) Simulation to hardware correlation for DT = 100 μ m, DK = 2.98, and DF = 0.004 for LCP core.

An interesting aspect of this new stack-up is the via transitions of transmission lines through isolating PP and GG segments. Unlike traditional PG segments, the current return path discontinuity would be small, as both transmission lines would be referenced to the same voltage plane.

A. Simulation to Measurement Correlation

The no-PG planes design has been implemented on a liquid crystalline polymer (LCP) board. For verification of measurements with simulations, we extracted the materials properties using simple shorted cavity resonators of size 4.05 cm \times 4.05 cm following the methodology in [12] and [13], as shown in Fig. 4. The extracted parameters for the LCP core were thickness of 100 μ m, dielectric constant of 2.98, and loss tangent of 0.004. Using the extracted parameters, the shorted cavity resonator was simulated with the full-wave simulator Sonnet [14]. Fig. 4 shows excellent match between simulation and measurement.

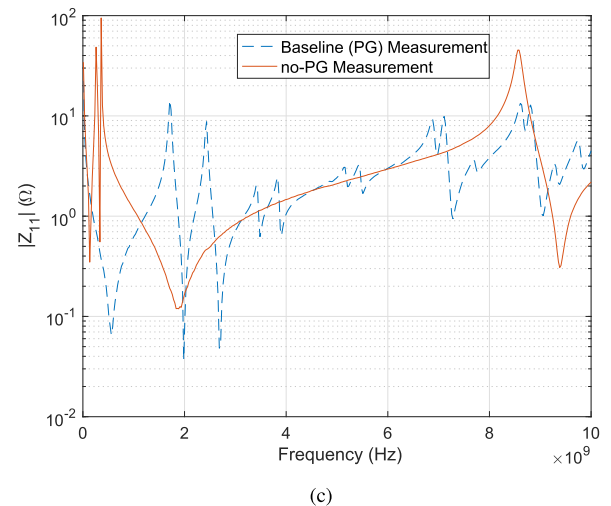
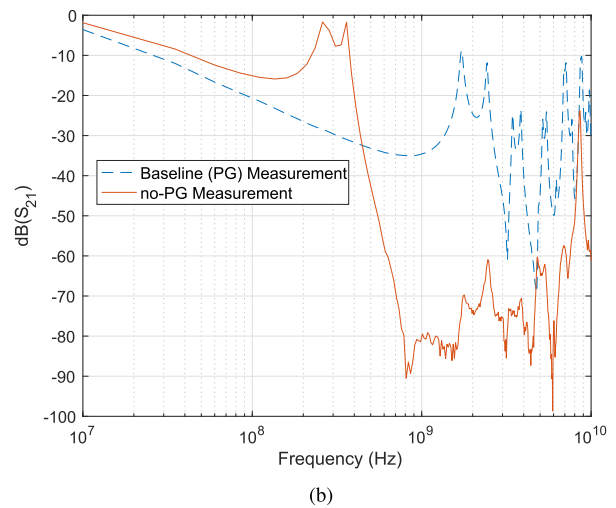
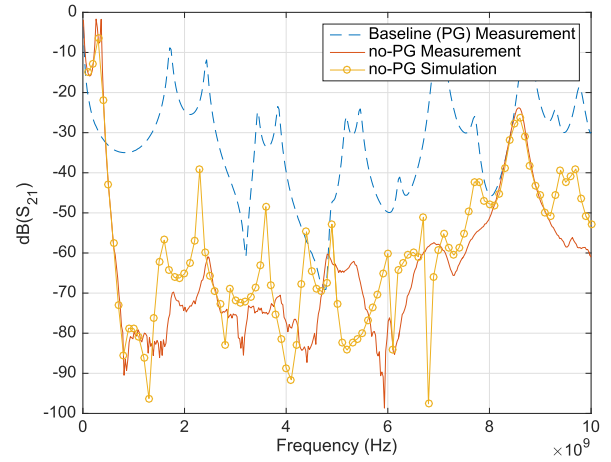


Fig. 5. (a) Simulation to hardware correlation for no-PG planes. Measurements indicate more than 50-dB isolation from 0.6 to 8 GHz for the no-PG design, eliminating the high level of coupling of the baseline case consisting of solid PG planes. (b) Same measurements plotted without the simulation data in logarithmic scale for clarity. (c) Measured input impedance of the no-PG design shows suppressed cavity resonances in its stopband.

We then used these extracted parameters to simulate the no-PG planes design in Fig. 3. The total size of the board is 5 cm \times 5 cm. Measurements were taken using microprobes

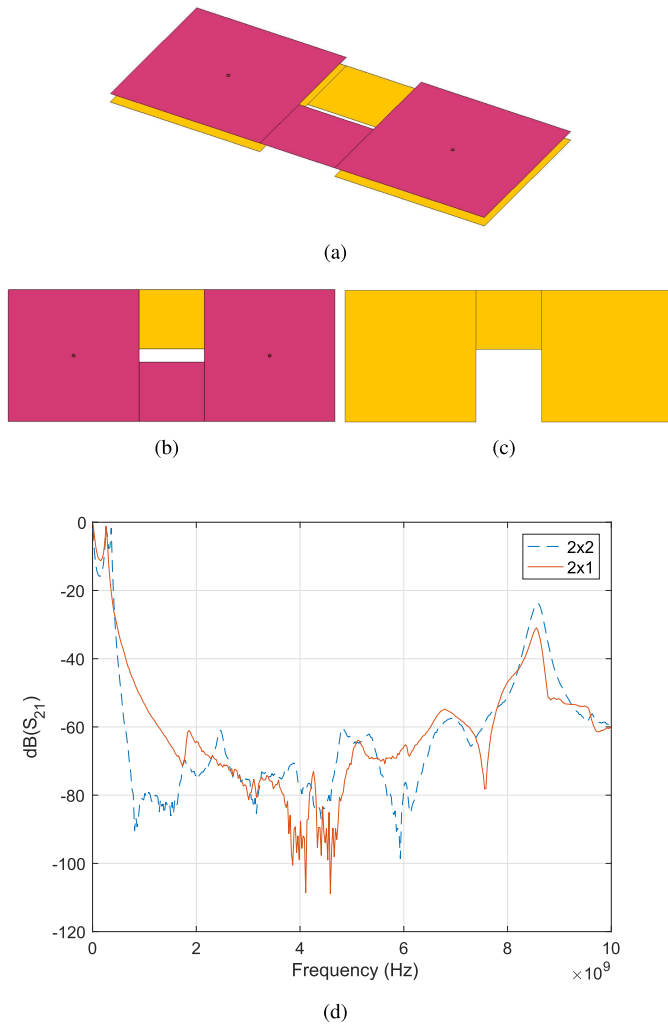


Fig. 6. Smaller board of size $5\text{ cm} \times 2\text{ cm}$ consisting of 2×1 segments. (a) 3-D view. (b) Top view. (c) Ground plane. (d) Measured isolation level is similar to the larger 2×2 board in Fig. 3.

by isolating the board from the measurement chuck using a 3-mm-thick plexiglass. Simulations predict accurately the on-set and off-set frequencies for the isolation bandwidth, as shown in Fig. 5(a). Measurements indicate more than 50-dB isolation from 0.6 to 8 GHz for the no-PG case, while there is a high level of coupling for the baseline case consisting of solid PG planes. This bandwidth for isolation is outstanding and typically not achievable using existing approaches, such as power islands/archipelago, electromagnetic bandgap structures, or virtual ground fence. As an example, the electromagnetic bandgap structure in [3] has 30-dB isolation from 1.76 to 9.72 GHz and may cause signal integrity problems due to return path discontinuity.

Outside of the isolation frequency band, the coupling could actually increase, as shown in Fig. 5(b), plotted again in logarithmic scale for better clarity. The crossover where the no-PG case has more isolation than the solid PG planes occurs at approximately 450 MHz. Fig. 5(c) shows the magnitude of the input impedance of the no-PG case, which suppresses the cavity resonances in its stopband. Its input impedance,

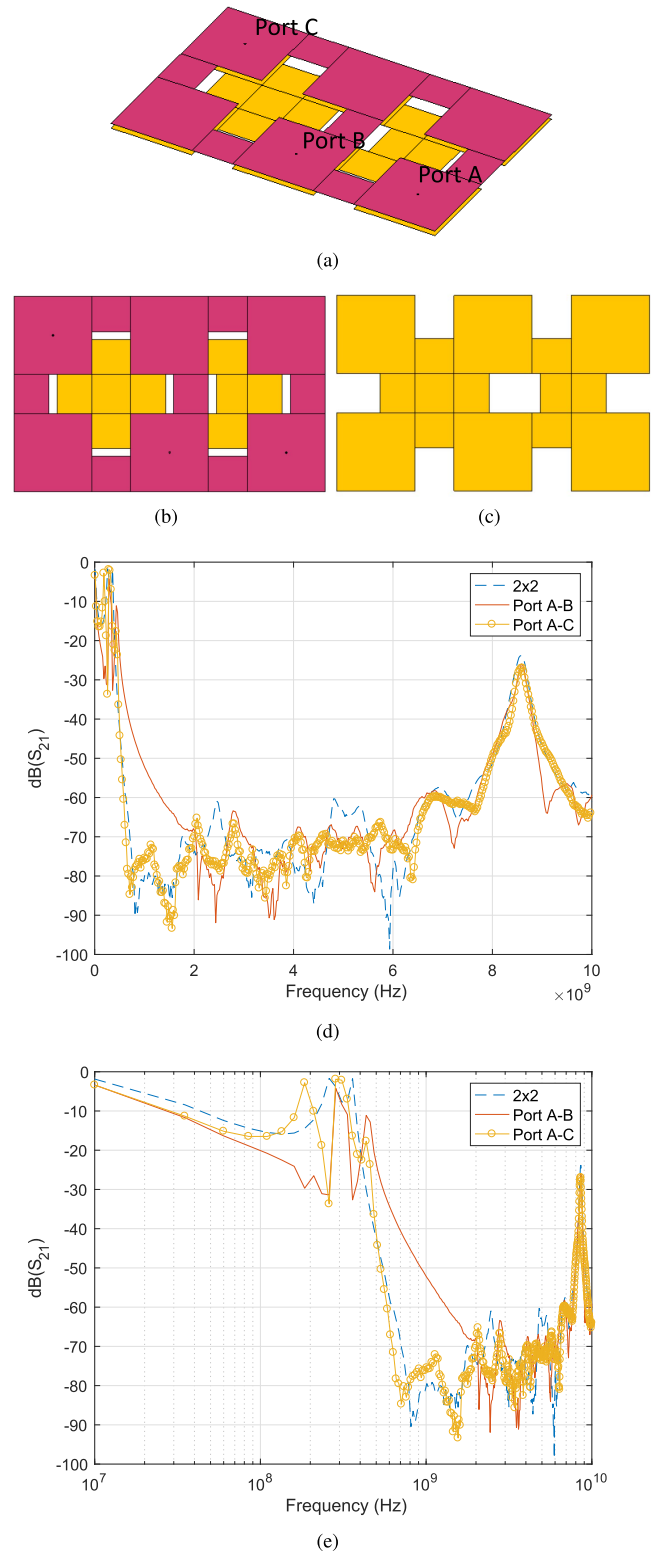


Fig. 7. Larger board of size $8\text{ cm} \times 5\text{ cm}$ consisting of 3×2 segments. (a) 3-D view. (b) Top view. (c) Ground plane. (d) Port location has primarily an impact on the on-set frequency of the stopband. (d) Same measurements plotted in logarithmic scale for clarity at lower frequencies.

however, exceeds the impedance of solid PG planes at lower frequencies. The test boards did not include any decoupling capacitors, which can address some of the coupling and increased impedance issues at these lower frequencies.

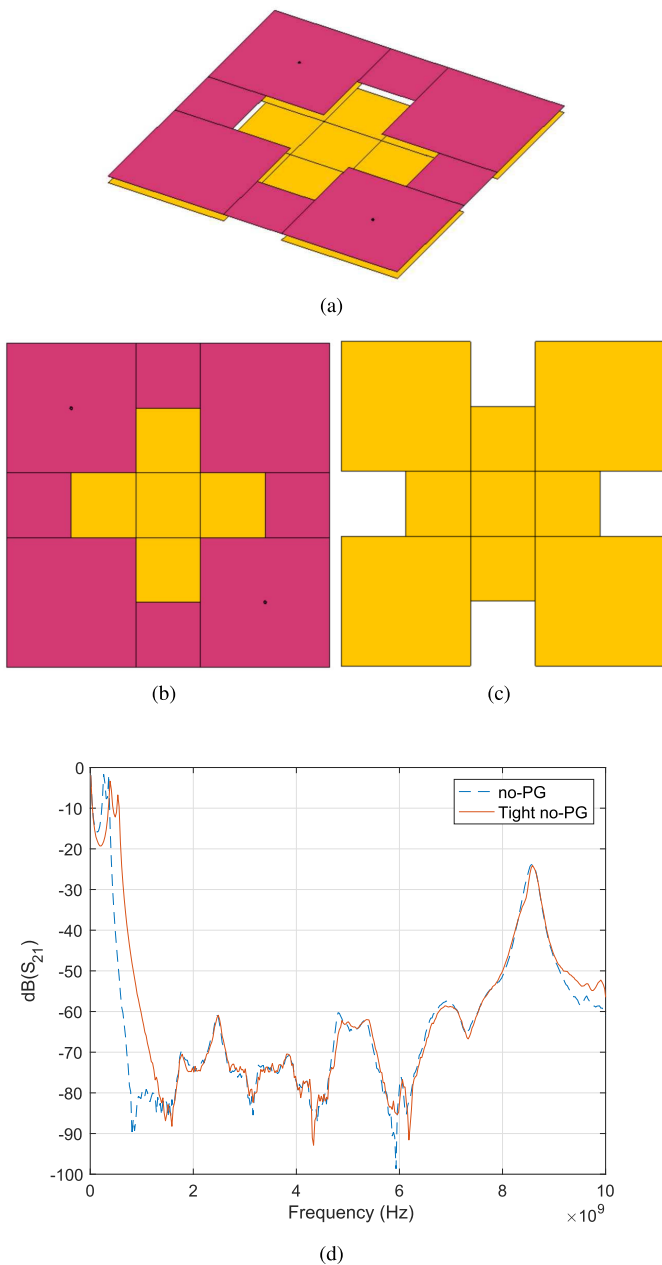


Fig. 8. Tight design of P and G segments with no gaps. (a) 3-D view. (b) Top view. (c) Ground plane. (d) Gap capacitance only has an impact on the measured on-set frequency of the stopband.

IV. DESIGN OPTIONS

The design of the no-PG planes is going to depend on the board size, port location, segment separation, segment size, and IR -drop considerations. Next, we investigate the impact of these parameters on the performance of the PG planes. The following results are the measurement data of the same test coupon in Section III.

A. Board Size

A rectangular-sized board of size $5\text{ cm} \times 2\text{ cm}$ is considered, as shown in Fig. 6. This design consists of 2×1 PG segments, and hence, the isolation is provided by a single isolating segment. However, the resulting isolation level is similar to the larger 2×2 board in Fig. 3. Unlike EBG designs that require

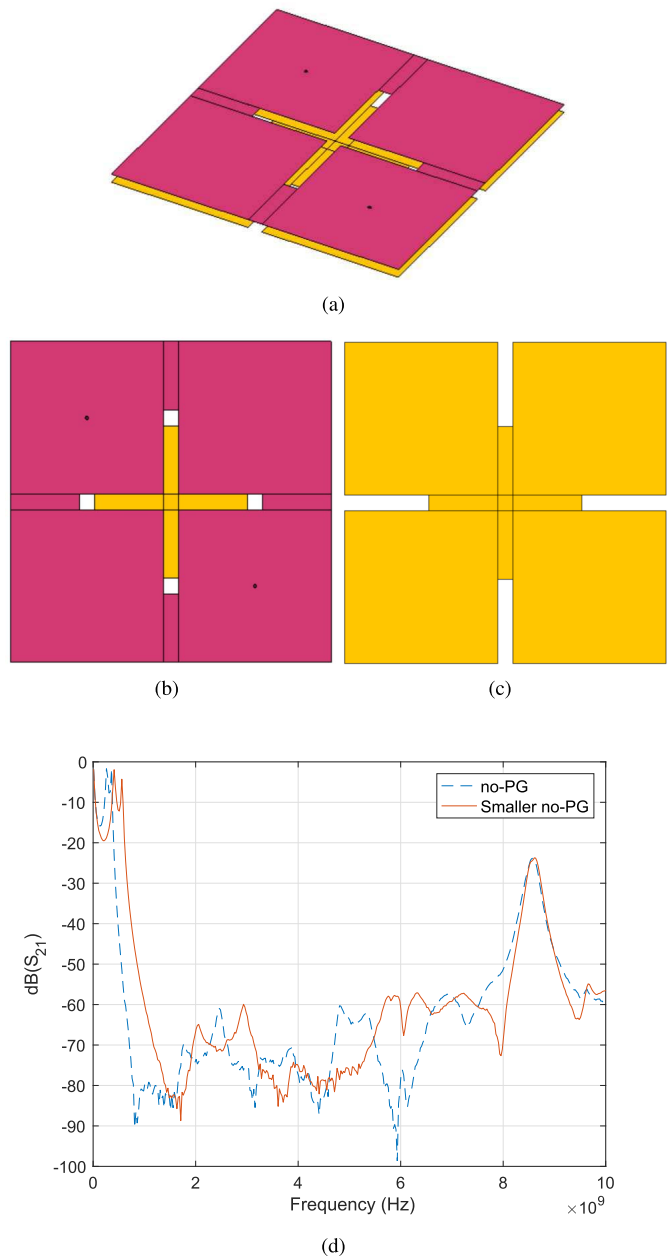


Fig. 9. Design with shorter isolating segments. (a) 3-D view. (b) Top view. (c) Ground plane. (d) Shorter segments primarily affect the measured on-set frequency of the stopband.

multiple unit cells to achieve high levels of isolation, this example demonstrates that a single isolating P and G segment is already effective to filter the power plane noise.

B. Port Location

A larger board of size $8\text{ cm} \times 5\text{ cm}$ with 3×2 PG segments is considered, as shown in Fig. 7. High isolation is achieved among various PG segments. The on-set frequency of the stopband is smaller when ports are farther from each other. In this case, the connection is achieved through multiple P and G segments. The measured off-set frequency of the stopband was similar for different port locations.

C. Segment Separation

There is an intentional gap between P and G segments in the no-PG design as seen from the top view in Fig. 3(c) to reduce

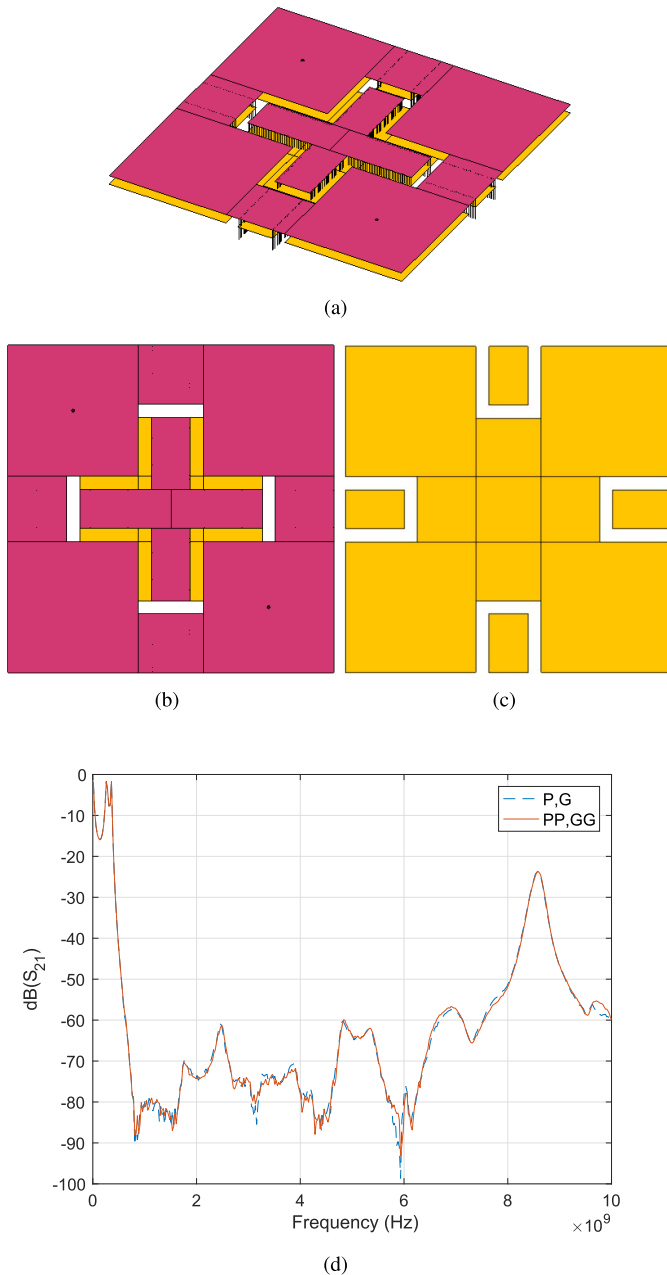


Fig. 10. Design with PP and GG segments to reduce IR -drop compared to the P and G segments in Fig. 3. (a) 3-D view. (b) Top view. (c) Ground plane including four small patches for power. (d) PP and GG segments should reduce IR -drop without affecting the high-frequency performance.

any parasitic gap capacitance from power to ground planes. To investigate the impact of this gap capacitance, a tight design is considered in Fig. 8, where the gaps have been removed. The results suggest that the gap capacitance only has an impact on the on-set frequency of the stopband, as shown in the figure.

D. Segment Size

The length of the isolating PP and GG segments can be made shorter if necessary. A modified design with smaller segments is considered in Fig. 9, where the overall size of the board has been reduced to 4.2 cm \times 4.2 cm due to the shorter isolating segments. The length of the isolating

sections primarily has an impact on the on-set frequency of the stopband, as shown in the figure.

E. Low IR -Drop

The lowest IR -drop would be achieved for solid PG planes. Due to the cut-outs in P and G segments, their IR -drop would double compared to the solid PG planes, assuming a tight design and neglecting current crowding. This increase will, however, not be as significant as the IR -drop through electromagnetic bandgap structures or power islands, which require narrow P segments. To further reduce IR -drop, PP and GG segments can be used as in Fig. 10 instead of P and G segments as in Fig. 3. The planes in PP and GG segments are shorted with each other using many vias. This provides a parallel current path for dc currents, which helps the IR -drop to approach that of solid PG planes, neglecting via resistance and current crowding effects. The presence of these vias and plane segments does not affect the high-frequency performance, as shown in Fig. 10.

To summarize, all considered design options provided similar isolation performance with the exception of the on-set frequency of the stopband, demonstrating the versatility of using no-PG planes.

V. CONCLUSION

An outstanding isolation level and bandwidth has been demonstrated using no-PG planes. This simple approach overcomes some of the major shortcomings of existing approaches for gigahertz power integrity as it does not require narrow power plane bridges that increase IR -drop and cause return path discontinuities. Isolation of gigahertz noise coupling through the PDN has been observed for various design options, indicating a robust design approach that does not require complex electromagnetic analysis. Segmenting the PG planes using this approach can allow localized PDN design, radically simplifying the current PDN design processes.

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Arif Ege Engin (M'05) received the B.S. degree in electrical engineering from Middle East Technical University, Ankara, Turkey, in 1998, the M.S. degree in electrical engineering from the University of Paderborn, Paderborn, Germany, in 2001, and the Ph.D. degree from the Leibniz University of Hanover, Hanover, Germany, in 2004.

He was a Research Engineer with the Fraunhofer-Institute for Reliability and Microintegration, Berlin, Germany. From 2006 to 2008, he was an Assistant Research Director with the Microsystems Packaging Research Center, Georgia Institute of Technology, Atlanta, GA, USA. He is currently an Associate Professor with the Electrical and Computer Engineering Department, San Diego State University, San Diego, CA, USA. He has over 100 publications in journals and conferences in the areas of signal and power integrity modeling and simulation and four patents. He is the coauthor of the book *Power Integrity Modeling and Design for Semiconductors and Systems* (Prentice-Hall, 2007) translated to Japanese and Chinese.

Dr. Engin was a recipient of the Semiconductor Research Corporation Inventor Recognition Award in 2009, the Outstanding Educator Award from the International Microelectronics Packaging and Assembly Society in 2015, and the Alexander-von-Humboldt Research Fellowship for 2015–2018.



Ivan Ndip (M'05–SM'12) received the M.Sc. and Ph.D. degrees (Hons.) (*summa cum laude*) in electrical engineering from the Technical University (TU) of Berlin, Berlin, Germany, in 2002 and 2006, respectively.

In 2002, he joined as a Research Engineer with the Fraunhofer-Institute for Reliability and Microintegration, Berlin. In 2005, he was appointed as the Group Manager of RF modeling and simulation. Six months later, he established the RF and High-Speed System Design Group, IZM, and served as the Founding Group Manager until 2015. From 2005 to 2015, he built up and led a dynamic team of research engineers and scientists. During this period of ten years, he led fundamental research projects, and industrial research and development projects, with national and international partners in the areas of measurement and analysis of dielectric materials in dependence on frequency and temperature; electromagnetic modeling, numerical simulation, measurement, and optimization of integrated antennas; high-frequency characterization and optimization of RF components, modules, and systems for signal/power integrity and intrasystem EMC; design of power-distribution networks and suppression of power-ground noise in mixed-signal modules, and RF system-integration of transceiver modules. Since 2014, he has been the Head of the Department of RF and Smart Sensor Systems, IZM. He has been a Lecturer with the School of Electrical Engineering and Computer Sciences, TU Berlin, since 2008. He also teaches professional development courses to practicing engineers and scientists worldwide. He has authored and coauthored over 150 publications in referred journals and conference proceedings.

Dr. Ndip is a member of the Technical Program Committee of many IEEE and IMAPS international conferences. He is a fellow and a Life Member of IMAPS. He was a recipient of six best paper awards at leading international conferences as well as a recipient of the Tiburtius-Prize, awarded yearly for outstanding Ph.D. dissertations in the state of Berlin. He was also a recipient of the 2012 Fraunhofer IZM Research Award for his work on the development and successful application of novel methods, models, and design measures for electromagnetic optimization of high-frequency and high-speed systems, and the 2016 John A. Wagnon Technical Achievement Award for his outstanding technical contributions to the microelectronics industry worldwide. He chairs the Signal and Power Integrity Committee of the International Microelectronics Assembly and Packaging Society. He was a Technical Co-Chair of the 44th and 45th International Symposiums on Microelectronics, Long Beach, CA, USA, and San Diego, CA, USA, in 2011 and 2012, respectively. In 2013, he was the Technical Chair of the 46th International Symposium on Microelectronics, Orlando, FL, USA, and in 2014, he became the General Chair of the 47th International Symposium on Microelectronics, San Diego, CA, USA. He also served as the General Chair of the 19th IEEE Workshop on Signal and Power Integrity (SPI 2015), Berlin. He is an Associate Editor for the *Journal of Microelectronics and Electronic Packaging*. He is also a reviewer of the IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY, the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, the IEEE TRANSACTIONS ON ELECTRON DEVICES, and other international journals.



Klaus-Dieter Lang (M'08–SM'13) received the M.Sc. (Dipl.-Ing.) degree in electrical engineering and Ph.D. degrees in wire bonding of multilayers and in quality assurance in assembly processes from Humboldt University (HU), Berlin, Germany, in 1981, 1985, and 1989, respectively.

In 1981, he joined HU as a Researcher, where he was involved in microelectronic assembly, packaging, and quality assurance until 1991. In 1991, he joined SLV Hannover, Hanover, Germany, to build up a department for microelectronic and optic components manufacturing. In 1993, he became the Department Manager for chip interconnections with Fraunhofer-Institute for Reliability and Microintegration (IZM), Berlin, where he was the Directors Personal Assistant from 1995 to 2000, and also responsible for marketing and public relations. From 2001 to 2005, he coordinated the Branch Lab Microsystem Engineering, Adlershof, Berlin. From 2003 to 2005, he was the Head of the Department of Photonic and Power System Assembly, and from 2006 to 2010, he was the Deputy Director of IZM. Since 2011, he has been the Director of Fraunhofer IZM and a Professor with the Technical University of Berlin. He is the author or coauthor of three books and over 130 publications in the field of wire bonding, microelectronic packaging, microsystems technologies, and chip on board.

Prof. Lang is a member of numerous scientific boards and conference committees, which include the Semiconductor Equipment and Materials International Award Committee and the Scientific Advisory Board of European Cluster of Electronic Packaging and Integration of Microdevices and Smart Systems, the Executive Board Member of VDE-GMM, and the Scientific Chair of the Conference Technologies of Printed Circuit Boards and SMT/HYBRID/PACKAGING. He is a member of the Deutscher Verband für Schweissen und verwandte Verfahren eV and the International Microelectronic Assembly and Packaging Society, and plays an active role in the international packaging community as well as in conference organization.



Gerardo (Jerry) Aguirre (M'96–SM'14) was born in El Paso, TX, USA, in 1960. He received the B.S. degree from the University of Texas at El Paso, El Paso, TX, USA, in 1983, and the M.S. and Ph.D. degrees from The University of Arizona, Tucson, AZ, USA, in 1986 and 1996, respectively, all in electrical engineering.

He was with the Antenna Development Division, Radar Department, Sandia Laboratories, Albuquerque, NM, USA; the Atmospheric Sciences Division, Los Alamos National Laboratories, Los Alamos, NM, USA; and the Electronics Package Group, Texas Instruments, Dallas, TX, USA. He is currently a member of the Technical Staff with the Product Technology Center, Kyocera International, Inc., San Diego, CA, USA. His current research interests include electrical performance of electronic packages and high-frequency properties of integrated circuit packages.