# Power Archipelago for Filtering Power Plane Noise

Arif Ege Engin, *Member, IEEE*, Chris Fergusson, Qian Fei Su, and Jerry Aguirre, *Senior Member, IEEE*

***Abstract*—Noise coupling in mixed-signal systems from shared power distribution networks (PDNs) can be a critical problem. Sensitive radio-frequency integrated circuits have to be isolated from voltage fluctuations caused by simultaneously switching drivers. This paper introduces the concept of the power archipelago, a new methodology for filtering the power plane noise. The power archipelago is essentially a lumped element microwave filter in which the discrete elements have been translated to embedded elements, effectively filtering out noise from the PDN. This paper demonstrates the increased isolation achieved by the power archipelago by hardware measurements and simulation correlations.**

***Index Terms*—Materials characterization, power and ground planes, power distribution network (PDN), power integrity, simultaneous switching noise.**

## I. Introduction

GIGAHERTZ noise is coupled from high-speed I/Os to the power distribution network (PDN) due to the return path discontinuities. This results in nonlocalized crosstalk among I/Os. Switching noise can also propagate through the power and ground planes to RF ICs, resulting in an increased noise figure. It is, therefore, critical to design the PDN considering the GHz spectrum. To achieve this, we propose a new design methodology for GHz power integrity, the power archipelago that is a filter for power plane noise.

Signal filters are ubiquitous components in high-frequency analog systems. Their design procedure is well-established, typically following impedance and frequency scaling of a prototype filter based on the insertion-loss method. With faster rise times and increasing clock and I/O speeds in digital systems, there is a growing need to apply microwave techniques in high-speed digital systems as well. A major bottleneck in designing robust high-speed digital systems is ensuring power integrity. This has been traditionally achieved by proper selection and placement of discrete decoupling capacitors on the IC package and printed circuit board. However, discrete decoupling capacitors do not effectively control voltage noise at GHz frequency. In this paper, we present for the first time a systematic approach to design a power filter for GHz power integrity. We demonstrate its design procedure on power/ground planes based on the insertion loss method.

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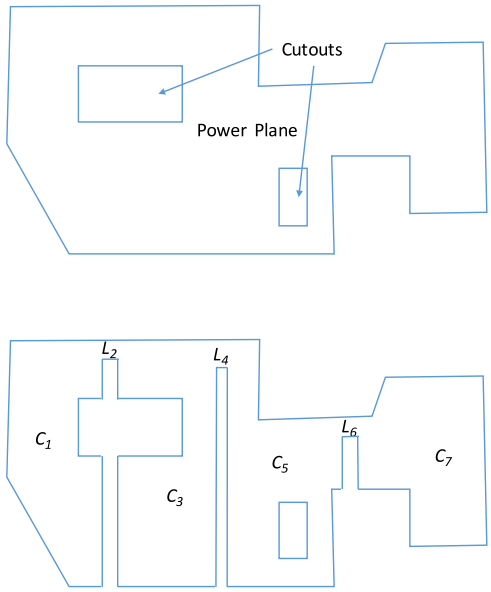


Fig. 1. Power archipelago (bottom) designed by segmenting the existing power plane (top).

Power archipelago is based on the power island concept [1], [2], but multiple power islands with carefully selected patch sizes and inductive bridges are used [3]. The basic structure of the power archipelago is a lumped element microwave filter with the discrete elements translated to embedded elements, realized in the power/ground plane geometry. The entire power plane then acts as a filter, isolating one side of the board from noise on the other side as shown in Fig. 1.

There are a number of existing methodologies for power plane filtering, and a good overview of those can be found in [4]. The shortcomings of two of the existing methodologies these with a similar function to the power archipelago are as follows:

1) Electromagnetic bandgap (EBG) structures: EBG structures are periodic structures used as filters on a power plane (e.g., [5]–[8]). A major issue with the practical application of EBG structures is the lack of design equations. Design equations for EBG structures exist for only specific EBG types [9]–[13]. In addition, it is difficult to have completely periodic EBG structures due to the presence of other board elements, such as cutouts, signal or stitching vias, which may alter the bandgap of the EBG structure [14].
2) Virtual ground fence (VGF): The VGF consists of quarter-wave transmission line stubs arrayed around the RF IC, which essentially acts as a Faraday cage to isolate the RF IC from noise in the environment [15]. VGF is a narrowband technique, due to being based on transmission line stubs of precise length.

TABLE I
ELEMENT VALUES FOR 7TH ORDER CHEBYSHEV TYPE-I LOW-PASS FILTER, $f_c = 1$ GHz, 10 Ω, 3DB RIPPLE

| $R_0$ ($\Omega$) | $C_1$ ($pF$) | $L_2$ ($nH$) | $C_3$ ($pF$) | $L_4$ ($nH$) | $C_5$ ($pF$) | $L_6$ ($nH$) | $C_7$ ($pF$) |
|---|---|---|---|---|---|---|---|
| 10 | 56.0 | 1.23 | 73.84 | 1.28 | 73.84 | 1.23 | 56.0 |

The power archipelago overcomes these shortcomings, as it is based on the insertion-loss method in microwave-filter design theory unlike the periodic structures in EBG filters. This makes the power archipelago broadband and easy to design with arbitrary shapes. An EBG signal filter making use of microwave-filter techniques has been described in [16]; however, the design of the power archipelago is based on filtering of an irregularly-shaped power plane. We make use of the property that the insertion loss in the passband and the system impedance are both irrelevant to the function of the power filter. It works equally well with a uniform board or an irregular board, and does not add cost to manufacture. We first introduced the power archipelago in [3], which demonstrated its performance as a function of filter impedance. In this paper, we extend the work in [3] by investigating the impact of other design variables, such as the filter type, order, and shape. We also provide hardware measurements of the power archipelago and simulation correlations by careful extraction of material properties considering surface roughness loss.

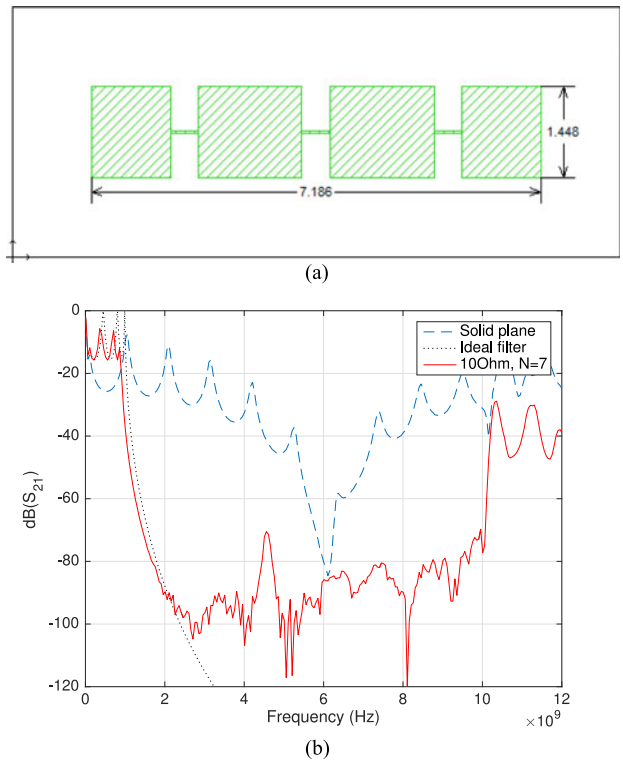


Fig. 2. (a) Power archipelago over solid ground plane, designed at $f_c = 1$ GHz with $R_0 = 10\ \Omega$ (units in cm). (b) Good agreement to insertion loss of ideal lumped element filter. Better than 70 dB isolation maintained using the power archipelago from 2 to 10 GHz.

## II. BASIC POWER ARCHIPELAGO DESIGN

The power archipelago example we choose is effectively a Chebyshev type-I (or equiripple) low-pass microwave filter that has been converted to a form usable in power plane geometries. A Chebyshev type-I low-pass filter consists of series inductors and shunt capacitors in a ladder circuit. These elements are approximated as microstrip lines and parallel plate capacitors, respectively, for use in the power archipelago. The basic structure of the power archipelago is some number of capacitive patches connected by inductive bridges over a solid ground plane, as shown in Fig. 1.

The values for the equivalent circuit elements used come from a prototype filter with normalized source impedance and cutoff frequency [17], scaled to the desired cutoff frequency and system impedance using

$$C_k = \frac{g_k}{R_0 \omega_c} \tag{1}$$

$$L_k = \frac{R_0 g_k}{\omega_c} \tag{2}$$

where $g_k$ are the values of the prototype filter, $R_0$ is the system impedance for the design, and $\omega_c = 2\pi f_c$ is the desired cutoff frequency. Table I shows the values for a filter designed with system impedance of $10\,\Omega$ at $f_c = 1$ GHz.

In order to convert these values to the dimensions required for the power archipelago, parallel plate capacitance and microstrip inductance formulas are employed. The power archipelago can also be implemented as a stripline design, where the power plane is sandwiched between two ground planes. In that case, stripline formulas should be used. For the capacitive patches, the area is found from the formula for parallel-plate capacitance

$$C = \frac{A\varepsilon}{h} \tag{3}$$

where $A$ represents area, $\varepsilon$ is the permittivity of the substrate, and $h$ is the thickness of the substrate. The per unit length inductance of the inductive bridges is as follows:

$$L_{\text{pul}} = \frac{Z_0 \sqrt{\varepsilon_{\text{eff}}}}{c} \tag{4}$$

where $\varepsilon_{\text{eff}}$ is the effective dielectric constant of a microstrip line and $c$ is the speed of light in a vacuum. Using the per unit length inductance value, the inductive bridges are then set to the appropriate lengths to provide the desired inductance for the filter.

To demonstrate the effectiveness of the power archipelago, a test structure is designed as shown in Fig. 2(a) based on the prototype filter in Table I. The stack-up consists of the low-loss dielectric RO4450F over a solid ground plane. Two ports at either end have been defined. Better than 70 dB isolation is maintained using the power archipelago from 2 to 10 GHz. As comparison, the solid plane case, with the well-known noise coupling issues due to resonances, is also shown. The behavior of the power archipelago closely matches that of the lumped

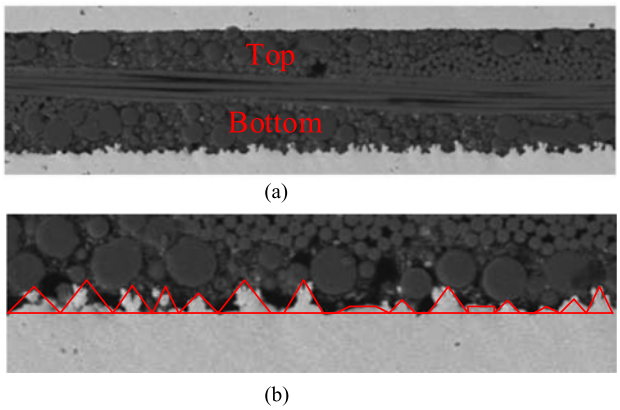


Fig. 3. (a) Cross section of dielectric reveals smooth top surface but rough bottom surface for the cavity. (b) A sample of the roughness of the bottom surface is fitted in simple geometrical shapes to calculate the rms value.

element filter around the onset frequency of the stopband, as can be seen in Fig. 2(b). The deviation is due to the parasitic elements not accounted for in the lumped capacitance and inductance implementation, losses in the power archipelago, and deviation of material properties from nominal values.

In comparing the solid plane case with the power archipelago, it is important to address practical aspects of implementation. Due to the introduction of narrow bridges, the IR drop increases and any transmission lines running over the slits experience return-path discontinuities. These are similar issues as in existing EBG implementations, and signal integrity issues can be reduced by using differential lines [18]. Due to the IR drop issue, the power archipelago or similar planar EBG implementations are most suitable when they are used to isolate an RF/analog chip, which does not consume much current, from a noisy digital circuit. The digital circuit can then be connected to the power supply with solid planes in consideration of IR drop. Another important aspect is the presence of vias and cutouts in a real board, which presents a challenge to maintain periodicity of a planar EBG structure. A power archipelago on the other hand can easily accommodate arbitrary plane shapes including via holes or cutouts as in Fig. 1 by adjusting the size of the patches, as it will be shown while discussing different filter shapes in this paper.

## III. Simulation to Hardware Correlation

To verify the measured data, the power archipelago was also simulated using the full-wave electromagnetic simulator Sonnet. The material properties play a critical role in accurate field simulation. To extract the electrical properties of conductors and the dielectric, cavity resonators have been measured following the methodology in [19], [20]. The geometrical properties were verified with cross section measurements as shown in Fig. 3. From Fig. 3(b), a sample of the roughness of the bottom surface is fitted in simple geometrical shapes to calculate the rms roughness value of the electrodeposited copper as 2.2 $\mu$m. The dielectric thickness was measured from the cross section in Fig. 3(a) as 91 $\mu$m (3.6 mil). The thickness was measured from the tip of the rough substrate, rather than the bottom of it, so

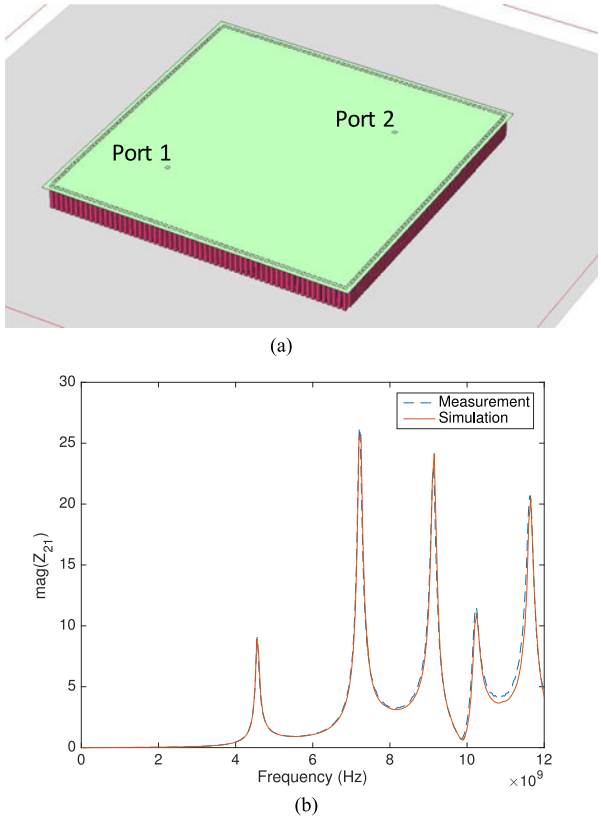


Fig. 4. (a) Simulated cavity resonator of size 2.36 cm × 2.36 cm (0.928″ × 0.928″) to extract dieletric constant and rms roughness. (b) Good agreement obtained with dielectric constant extracted as 3.82; the loss tangent as 0.0037; and the rms surface roughness of the bottom surface as 1 $\mu$m.

the dielectric is effectively thinner than the nominal 102 $\mu$m (4 mil) specified.

The cavity design of size 2.36 cm × 2.36 cm (0.928″ × 0.928″) is shown in Fig. 4(a). The material properties were fitted to simulations until a good match was found between simulation and measurements as shown in Fig. 4(b). The dielectric constant was extracted as 3.82; the loss tangent value was used from the datasheet as 0.0037; and the rms surface roughness of the bottom surface was extracted as 1 $\mu$m. The smaller rms value used in the simulator provided a better fit than the 2.2 $\mu$m rms value calculated from the cross section. This may be related to the inaccuracy of calculating the rms value from the cross section. Therefore, in the following simulations, a 1 $\mu$m rms value for surface roughness has been used.

Fig. 5 shows good agreement between simulation and measurement results for the power archipelago as well as the solid power plane by using the extracted parameters. The feature selective validation technique [21] has provided a GDM measure of "good" for the solid power plane case; and "fair" for the power archipelago in terms of simulation to hardware correlation.

## IV. Design Variables for Power Archipelago

In the following, we investigate the impact of system impedance, filter type, filter order, and filter shape on the performance of the power archipelago.

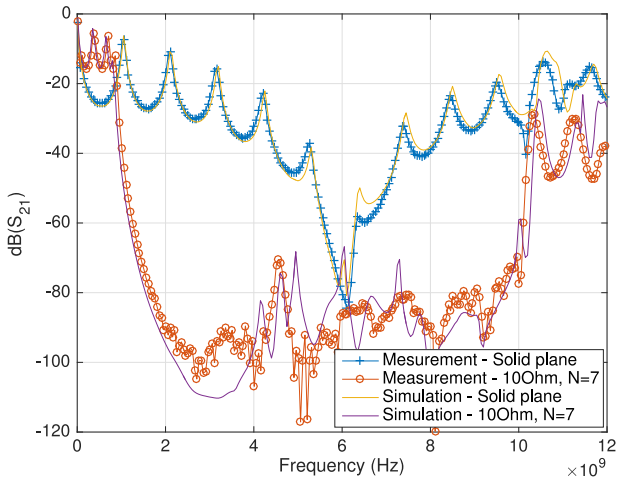


Fig. 5. Good agreement between simulation and measurement for power archipelago and solid power plane.

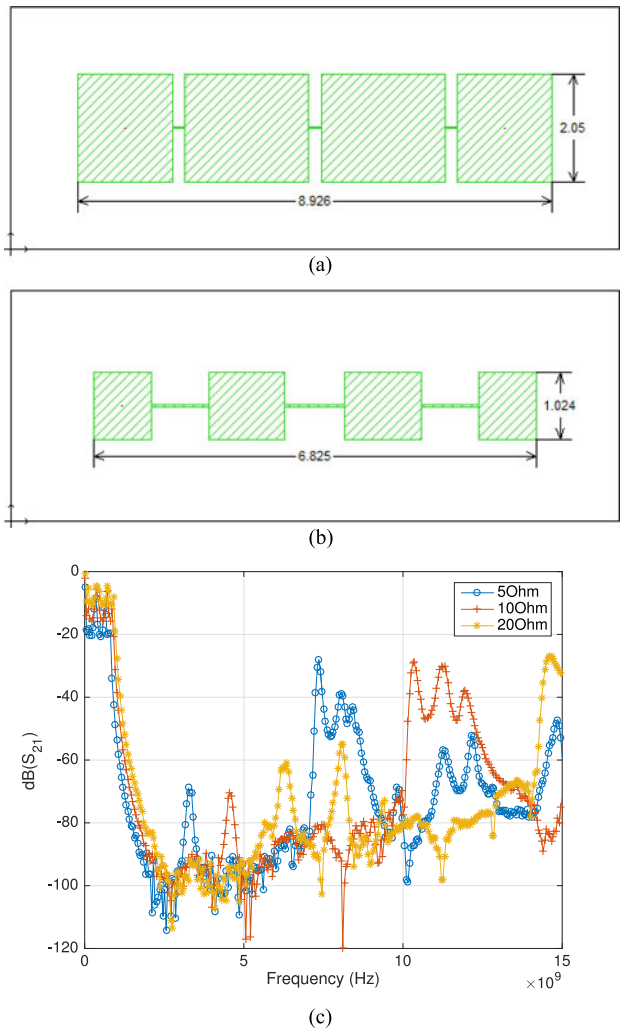


Fig. 6. Power archipelago over solid ground plane, designed at (a) $R_0 = 5\,\Omega$ and (b) $R_0 = 20\,\Omega$ (units in cm). (c) Measured insertion loss for power archipelago with various system impedances.

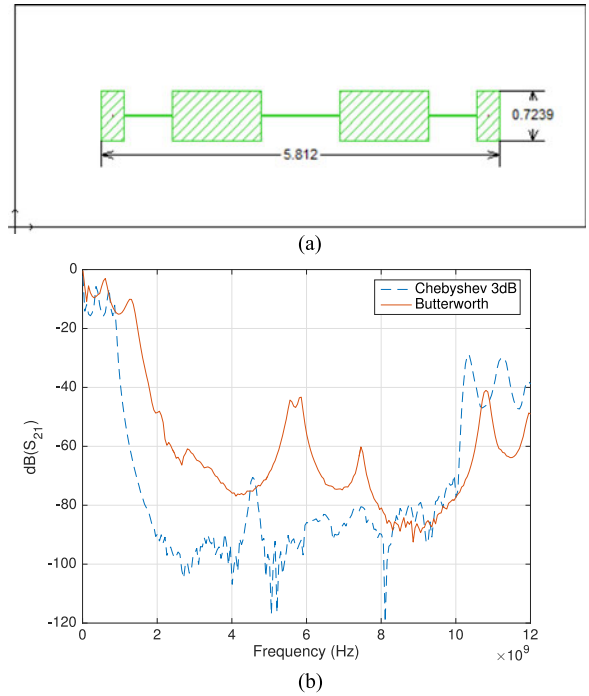


Fig. 7. (a) Butterworth type filter designed for $R_0 = 10\Omega$ and $N = 7$ (units in cm). (b) Measurements indicate that a similar Chebyshev type filter is superior in performance.

### A. *System Impedance*

The passband performance is not relevant in a power filter; therefore, impedance matching is not necessary. The length of the inductive bridges and surface area of the capacitive patches can be adjusted by choosing a different system impedance. Fig. 6 shows the differences in sizes for power archipelago designed for 5 and 20 Ω. The insertion loss of the power archipelago can be seen in Fig. 6(c). The insertion loss in all figures in this paper have been calculated with a reference of 50 Ω to provide a consistent comparison. In the passband, any increase in insertion loss is irrelevant in power filtering. The power archipelago behaves similarly in terms of the cutoff frequency; therefore, Fig. 6(c) demonstrates that the on-set frequency of the stopband can be accurately set using the insertion-loss method. The power archipelago is designed as a low-pass filter; however, ripples in the stopband or pseudo-passbands are observed. This limitation is due to the higher-order resonances of the patches. As an example, the largest patch of the 10 Ω filter has the lowest-order resonance at 4.6 GHz, which is observed as a ripple in the stopband. It can be observed that smaller patch sizes provide a larger stopband; therefore, using thinner dielectrics, and hence smaller capacitive patches, would improve the bandwidth.

Being able to design for various system impedances provides a free variable when an existing power plane is being segmented as in Fig. 1. This allows to calculate the proper system impedance to fit the power archipelago to the board.

### B. *Filter Type*

Since passband performance is irrelevant in the power archipelago, it is preferable to use the Chebyshev type filter

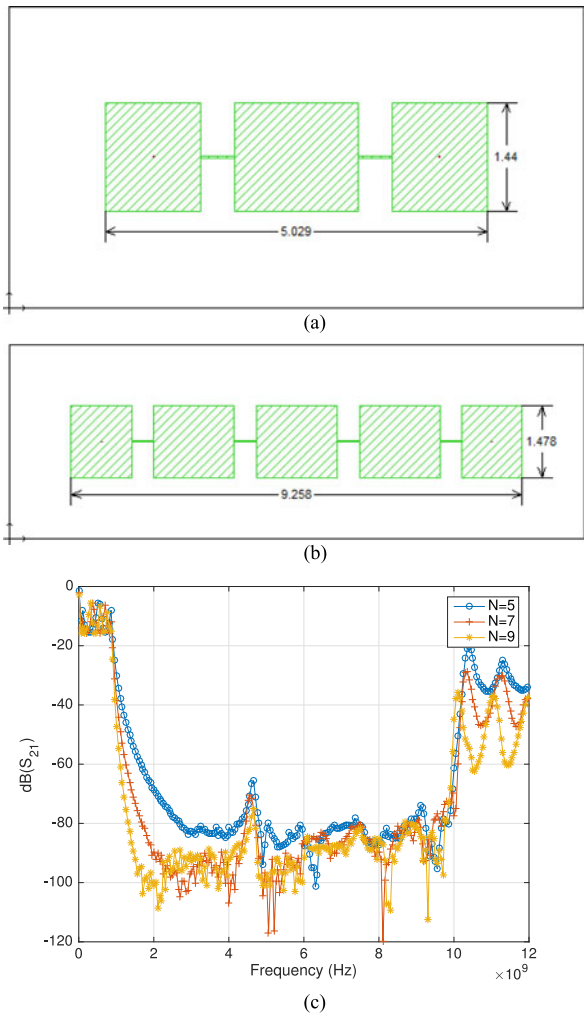


Fig. 8. Power archipelago over solid ground plane, designed at (a) $N = 5$ and (b) $N = 9$ (units in cm). (c) Measured insertion loss for power archipelago with various filter orders.

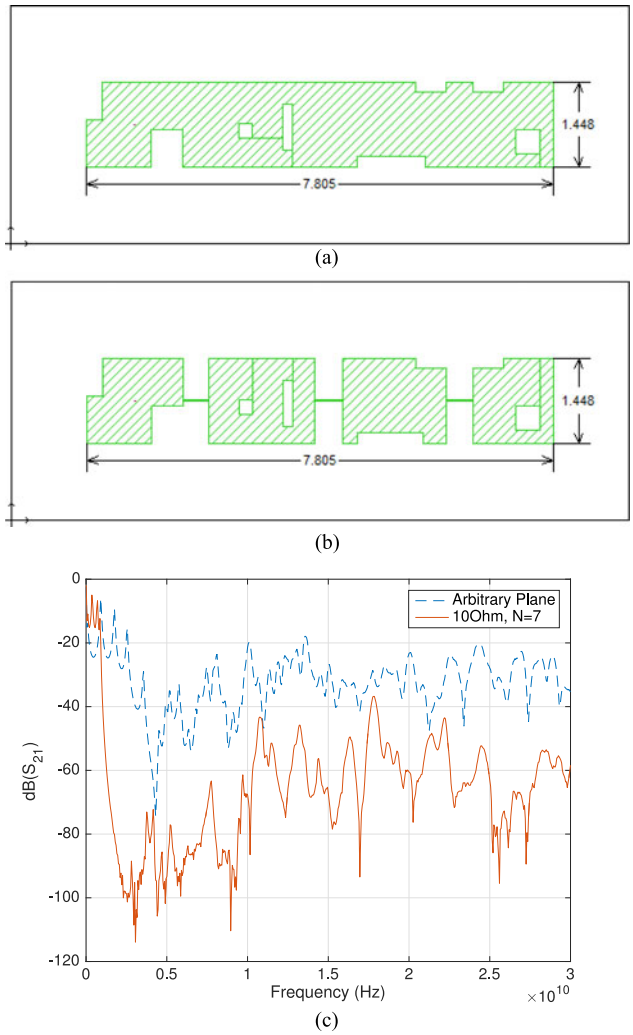


Fig. 9. Arbitrary power plane in (a) is used to form a power archipelago in (b) (units in cm). (c) Measured insertion loss for power archipelago shows improvement in isolation at all frequencies after cutoff frequency of the filter.

to provide a steeper cutoff response compared to Butterworth type. Also, Chebyshev filters with larger ripples in the passband can be preferred. To provide a comparison, a Butterworth type filter is also characterized and compared with the 3 dB Chebyshev filter in Fig. 7. Measurements validate that a similar Chebyshev type filter is superior in performance compared to the Butterworth type. The ripples in the passband of the Butterworth filter is due to the impedance mismatch, since the filter is designed for $R_0 = 10\,\Omega$ but the insertion loss in the figure is displayed for a reference impedance of $50\,\Omega$.

### C. Filter Order

Another variable in the design of the power archipelago is the order of the filter. Fig. 8 shows the differences in sizes for power archipelago designed for $N = 5$ and $N = 9$. In all cases, $R_0 = 10\,\Omega$ and a 3 dB Chebyshev type filter is implemented. There is no substantial improvement in the bandwidth of the stopband; therefore, a lower order filter may be preferred for convenience of application especially in small boards. However, the insertion loss in Fig. 8(c) shows that the isolation can be increased with the filter order. The required isolation level would depend on the amount of voltage noise on the board, as well as the characteristics of the circuits. To provide an example, a low-noise amplifier was tested in [15] in the presence of noise that was a pseudorandom bit sequence with a full voltage swing of 100 mV applied between the power and ground planes. The measured noise figure for this particular example could be maintained at its specified value when the isolation level was approximately 40 dB.

### D. Filter Shape

The power archipelago functions on irregularly shaped boards as well, provided the area of each capacitive patch is chosen as in the regular case. This means that the use of the power archipelago is practical, as the design can start with an existing power plane design, modified to have the necessary capacitive patches and inductive bridges. As an example, the irregularly shaped plane in Fig. 9(a) has been broken into capacitive patches and inductive bridges in Fig. 9(b). The overall size of the power

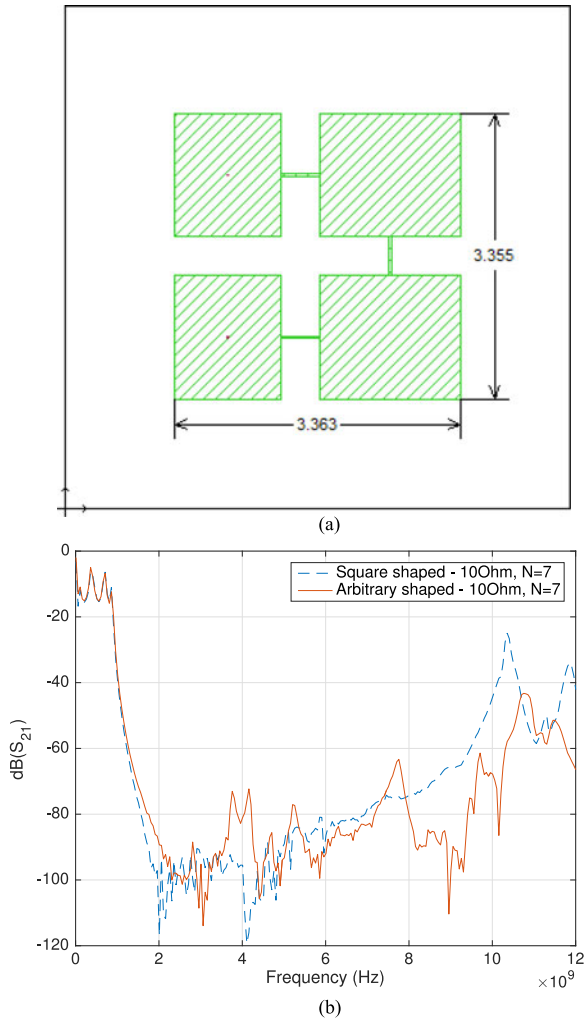


Fig. 10. (a) Power archipelago implemented on a square-shaped power plane (units in cm). (b) Measured insertion loss for power archipelago shows very similar response for two different board geometries.

plane has not been changed. The substantial increase in isolation from the irregular plane is observed in Fig. 9(c) from 2 GHz up to about 10 GHz. The isolation provided by the power archipelago also continues to be better up to 30 GHz.

As another example, a square-shaped board is shown in Fig. 10(a). The power archipelago has been designed to the same specifications as in the irregularly-shaped case in Fig. 9(b). The two power archipelago designs are compared in Fig. 10(b). A similar behavior in the cutoff frequency and bandwidth of these two different board designs can be observed, which demonstrates the simple design approach of power archipelago for a given arbitrary board.

## V. Conclusion

This paper introduced the power archipelago, which can effectively filter high-frequency PDN noise generated by digital circuits. The power archipelago consists of capacitive patches connected by inductive bridges, cut into the power plane, which mimic a low-pass filter. The measurements and simulation correlations demonstrate the noise reduction that can be achieved through this simple methodology.

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