This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

Passive Multiport *RC* Model Extraction for Through Silicon Via Interconnects in 3-D ICs

A. Ege Engin, *Member, IEEE*

***Abstract*—Parasitic *RC* behavior of VLSI interconnects has been the major bottleneck in terms of latency and power consumption of ICs. Recent 3-D ICs promise to reduce the parasitic *RC* effect by making use of through silicon vias (TSVs). It is therefore essential to extract the *RC* model of TSVs to assess their promise. Unlike interconnects on metal layers, TSVs exhibit slow-wave and dielectric quasi-transverse-electromagnetic modes due to the coupling to the semiconducting substrate. This TSV behavior can be simulated using analytical methods, 2-D/3-D quasi-static simulators, or 3-D full-wave electromagnetic simulators. This paper describes a methodology to extract parasitic *RC* models from such simulation data for interconnects in a 3-D IC.**

***Index Terms*—Macromodeling, passivity, *RC* model, through silicon vias (TSVs).**

I. Introduction

Accurate extraction of *RC* models are critical in time-domain simulation of interconnects to analyze latency, power consumption, and noise coupling. These electrical properties of interconnects have been the bottleneck in performance improvement based on CMOS scaling [1]–[3]. Recent 3-D ICs promise to reduce the parasitic *RC* effect by making use of through silicon vias (TSVs) [4], [5]. It is therefore essential to extract the *RC* model of TSVs to assess their promise. This paper presents a new macromodeling approach to extract an *RC* model not only for TSVs, but also other *RC* interconnect segments such as microbumps and redistribution layers in a 3-D IC.

The inductance of 3-D IC interconnects can also become an important parameter as the frequency increases. It has been reported that signal integrity is affected by the inductance above 10 GHz in 3-D ICs [6] and even at lower gigahertz regime for power integrity [7]. However, reducing the *RC* time-constant of the channel is considered the primary design factor for a high-speed TSV channel [8] as well as silicon interposers [9]. Closed-form expressions for TSV parasitic models have been studied in [10]–[17], where a specific geometry, such as a circular or square cross-section for TSVs, is assumed. Recently, an analytical equivalent circuit model was presented for coupled TSV structures in a 3-D IC [18]. This model accurately captured the transition between slow-wave and dielectric quasi-TEM modes, which are characteristic for metal–insulator–semiconductor transmission lines, as well as the MOS capacitance. The analytical approach in [18] is applicable to circular TSVs that have a 2-D field behavior. The approach in this paper allows to generate an *RC* model for arbitrary-shaped TSVs in the presence of other 3-D interconnect structures and substrate contacts.

Two different methodologies are presented to extract an *RC* model for 3-D IC interconnects:

1) *Model Fitting:* The analytical model in [18] works for circular TSVs that are placed at a large pitch compared to the TSV radius. For noncircular or closely spaced TSVs, a 2-D electric current simulation can provide the frequency-dependent admittance parameters. The topology of the original analytical model can still be used by fitting the capacitances and conductances in this model to the simulation results.
2) *RC Vector Fitting:* The topology of the analytical model is not adequate to model more complicated structures, such as when the redistribution layers are taken into account. The admittance data can be provided by the 3-D electric current or full-wave electromagnetic simulators, or even by measurements. This paper presents a general purpose multiport *RC* vector-fitting algorithm to extract an equivalent circuit model. This approach for the first time solves the problem of efficiently generating passive macromodels for 3-D IC interconnects. A one-port solution for this problem has been presented in [19]. In this paper, the *RC* macromodeling methodology is extended for multiport networks.

The model fitting methodology is customized for TSV arrays, so its application is limited to vertical interconnects in 3-D ICs. The *RC* vector-fitting approach, on the other hand, is a general macromodeling approach for all interconnect structures whose behavior can be approximated by an *RC* network. Both approaches are applicable when the inductance effects are negligible.

II. Model Fitting

Fig. 1 shows an *RC* model for circular TSVs, whose elements can be calculated using an analytical approach. The analytical model would however not be applicable in many cases, such as when the TSVs are square-shaped rather than circular. It would, however, be safe to assume that the same equivalent circuit topology as in Fig. 1 can adequately be used as a model. In this case, a 2-D electric current simulation can be performed to

Manuscript received February 11, 2013; revised August 4, 2013; accepted December 3, 2013. This work was supported by the U.S. Air Force Research Laboratory/Information Directorate, Rome, NY.

The author is with the Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA 92182 USA (e-mail: aengin@mail.sdsu.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TEMC.2013.2295049

0018-9375 © 2014 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

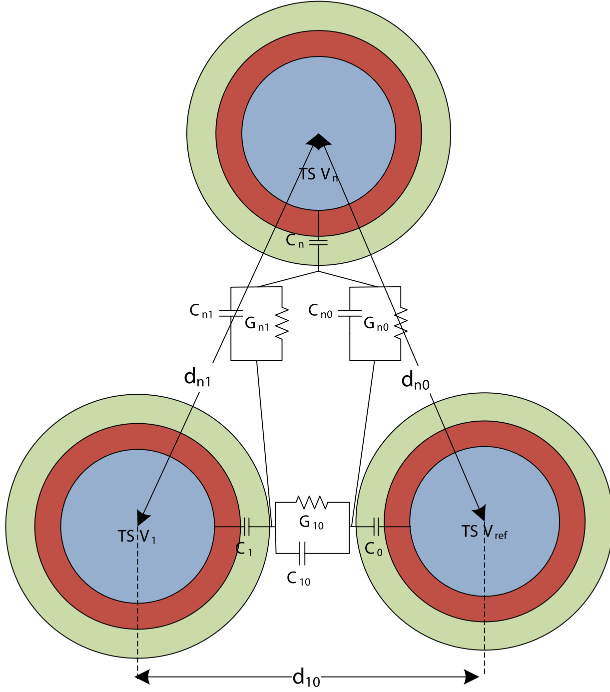


Fig. 1. Capacitance and conductance model for multiple coupled TSVs. The circles represent the metal via, dielectric liner, and the depletion region from inside out.

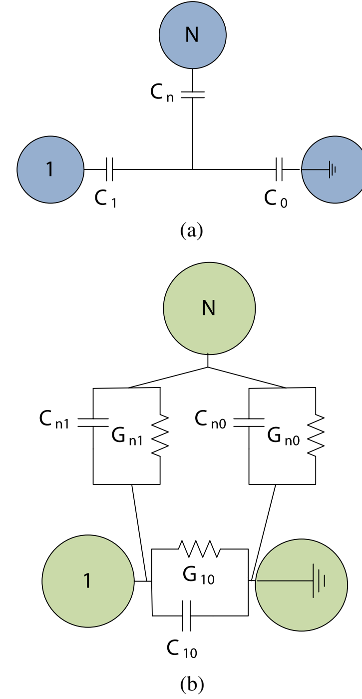


Fig. 2. (a) Low frequency model for the TSV array in Fig. 1. (b) Remaining part of the model after the low-frequency portion of (a) has been deembedded.

extract the per unit length admittance matrix of the configuration. The model in Fig. 1 then can be fitted to this admittance matrix. Model fitting approach refers to fitting this model to simulated or measured data. Model fitting approach also works when there are multiple ground TSVs randomly distributed in the TSV array.

One low-frequency and one high-frequency simulation are needed to uniquely extract all the circuit elements for an array with any number of TSVs. The low-frequency data are used to extract the side-wall capacitances (C_i), whereas the high-frequency data is used to extract the substrate capacitance and conductance (C_{ij}, G_{ij}).

Assume that the admittance matrix is provided at a very low frequency $\overline{\overline{Y}}_l$ and at a very high frequency $\overline{\overline{Y}}_h$. At the very low frequency point, all other parameters are neglected compared to the large impedance of the oxide capacitance C_i, hence, we obtain the model shown in Fig. 2(a). Note that this results in a T-model; therefore, it is more convenient to work with the impedance matrix to extract the oxide capacitances C_i. The impedance matrix of the model in Fig. 2(a) can be found as

$$\overline{\overline{Z}}_{ox} = \begin{bmatrix} Z_1 + Z_0 & Z_0 & \cdots & Z_0 \\ Z_0 & Z_2 + Z_0 & \cdots & Z_0 \\ \vdots & \ddots & \ddots & \vdots \\ Z_0 & Z_0 & \cdots & Z_N + Z_0 \end{bmatrix} \quad (1)$$

where $Z_i = 1/(j\omega C_i)$. All the off-diagonal terms in $\overline{\overline{Z}}_{ox}$ are equal to Z_0, the impedance of the ground TSV oxide capacitance (in addition to any depletion capacitance). Hence, the simulated admittance matrix is inverted to obtain $\overline{\overline{Z}}_l = \overline{\overline{Y}}_l^{-1}$ at the lowest frequency. Since the model in Fig. 2(a) is approximate, there will be small discrepancies between the off-diagonal elements of $\overline{\overline{Z}}_l$. Therefore, the average of all the off-diagonal terms can be taken to obtain C_0. The remaining oxide capacitances are obtained from the diagonal terms.

Next, the simulation data obtained at high frequency are used. The oxide capacitances are deembedded from the model in Fig. 1 resulting in the deembedded model as shown in Fig. 2(b). The deembedding can also be done most conveniently in terms of the impedance matrix as

$$\overline{\overline{Z}}_{Si} = \overline{\overline{Z}}_h - \overline{\overline{Z}}_{ox} \quad (2)$$

where $\overline{\overline{Z}}_{Si}$ is the impedance matrix of the model in Fig. 2(b). In (2), $\overline{\overline{Z}}_{ox}$ is calculated at the high frequency point. Since Fig. 2(b) corresponds to a π-model, it can be most conveniently represented in terms of its admittance matrix as

$$\overline{\overline{Y}}_{Si} = \begin{bmatrix} \sum_{i=1}^{N} Y_{1i} & -Y_{12} & \cdots & -Y_{1N} \\ -Y_{21} & \sum_{i=1}^{N} Y_{2i} & \cdots & -Y_{2N} \\ \vdots & \ddots & \ddots & \vdots \\ -Y_{N1} & -Y_{N2} & \cdots & \sum_{i=1}^{N} Y_{Ni} \end{bmatrix} \quad (3)$$

where the branch admittances are given by

$$Y_{ij} = Y_{ji} = G_{ij} + j\omega C_{ij}. \quad (4)$$

Hence, once the impedance matrix $\overline{\overline{Z}}_{Si}$ using (2) is obtained at the high frequency point, we can take its matrix inverse and

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

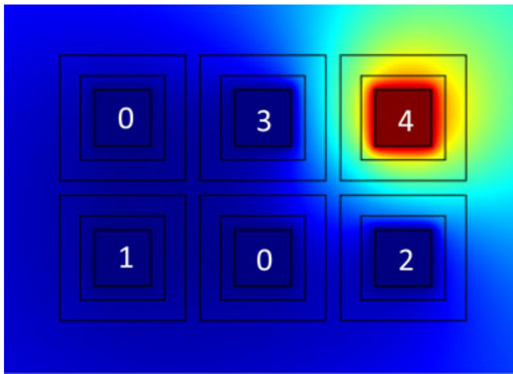


Fig. 3. Voltage distribution when the top right square-shaped TSV is kept at 1V, while all the other TSVs are grounded.

uniquely extract all the silicon conductances and capacitances using (3).

A. Numerical Example

This method has been applied on six coupled TSVs as shown in Fig. 3. The TSVs have the following parameters:

1) Pitch $= 5\,\mu$m,
2) TSV side length $= 2\,\mu$m,
3) Oxide thickness $= 0.5\,\mu$m,
4) Depletion width $= 0.74\,\mu$m,
5) Silicon permittivity $= 11.9$,
6) Silicon conductivity $= 10$ S/m,
7) SiO_2 permittivity $= 3.9$.

Fig. 3 shows the voltage distribution when the top right TSV is kept at 1V while all the other TSVs are grounded. The admittance matrix was extracted for the port assignment shown in the figure. Two of the TSVs where assigned to ground, whereas there were four signal TSVs. The simulations were done using a 2-D quasi-static simulator (the electric current module in COMSOL [20], which calculates per unit length admittance parameters of 2-D structures). An electric insulation boundary condition has been used, which enforces that the current density is parallel to the outside boundaries (i.e., there is no outward flow of the displacement current from the simulation boundaries).

Fig. 4 shows the admittance parameters related to TSV 2 as an example. The model was generated by using the simulation data at only the lowest and highest frequency points. A very good agreement to simulation was obtained following the presented model fitting methodology. The extracted model was also checked for passivity. The obtained circuit model included negative capacitances and conductances. However, the overall model was observed to be passive, since all eigenvalues of the capacitance and conductance matrix were positive.

III. Single-Port *RC* Vector Fitting

Postlayout simulation typically requires more accurate data that capture 3-D coupling effects including the parasitic coupling to metal layers, microbumps, and active circuits. An example is shown in Fig. 5, where the redistribution layers and a substrate contact is included in addition to the TSVs. In this case, there are more coupling paths than the simple electrical model in Fig. 1 suggests, so the model fitting approach in previous section may not be accurate. A more general approach for extracting a macromodel of the interconnects is required, where the circuit topology is not fixed.

This paper introduces the *RC*-vector fitting approach that has been previously used for generating Debye models of arbitrary order for organic and ceramic dielectric materials [21]. The basic method provides a guaranteed passive *RC* model for a one-port network. Table I provides a snapshot of this new algorithm compared to the standard vector fitting algorithm [22]. The standard vector fitting algorithm does not guarantee passivity, and generates a general *RLC* model. On the other hand, macromodels that are not passive may result in unstable time-domain responses [2]. Hence, ensuring passivity is critical in the generated model. The general approach for creating a passive model is by perturbing either the poles or residues of the nonpassive model until a passive response is obtained [23]–[25]. These iterative methods are not guaranteed to converge. A different approach in [26] generates a passive RLC model by construction, rather than by perturbation. This method relies on a sufficient but not necessary condition for passivity enforcement on RLC networks. Therefore, the obtained result may not be optimum. The *RC* vector fitting approach presented in this paper is not iterative and is based on the enforcement of passivity with sufficient and necessary conditions. Hence, for the first time, it allows to efficiently calculate residues that provide an optimum fit in the least-squares sense. Existing macromodeling methods for *RC* networks are generally model order reduction techniques, such as [27], hence are not suitable as a vector fitting algorithm to generate an *RC* network from tabulated data.

In the first step of the *RC* vector fitting approach, real stable poles are used as the initial poles in the standard vector fitting algorithm. For the examples considered, this results in relocated poles that are also real and stable if the order of the model is not higher than necessary. Hence, if complex or nonstable poles are generated, the order of the model can be reduced, or such poles can be discarded.

In the second step, residues are extracted. The partial fraction expansion of the impedance of an *RC* network can be expressed as

$$Z_{RC} = a + \sum_{i=1}^{N} \frac{k_i}{s - p_i} \tag{5}$$

where the constant term a and all residues k_i are positive, whereas all poles p_i are negative. This is a necessary and sufficient condition for the extracted rational function to represent the impedance of an *RC* network. Hence, the constant term and residues can be extracted using nonnegative least squares to ensure that the resulting model will represent an *RC* network.

Admittance parameters can also be used directly; however, the residues will be negative for the admittance of an *RC* network (e.g., a series *RC* branch has an admittance of $1/R - [1/R^2C]/[s + 1/RC]$). In general, admittance of an *RC* network (i.e., Y_{RC}) has positive a but negative residues k_i [28].

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

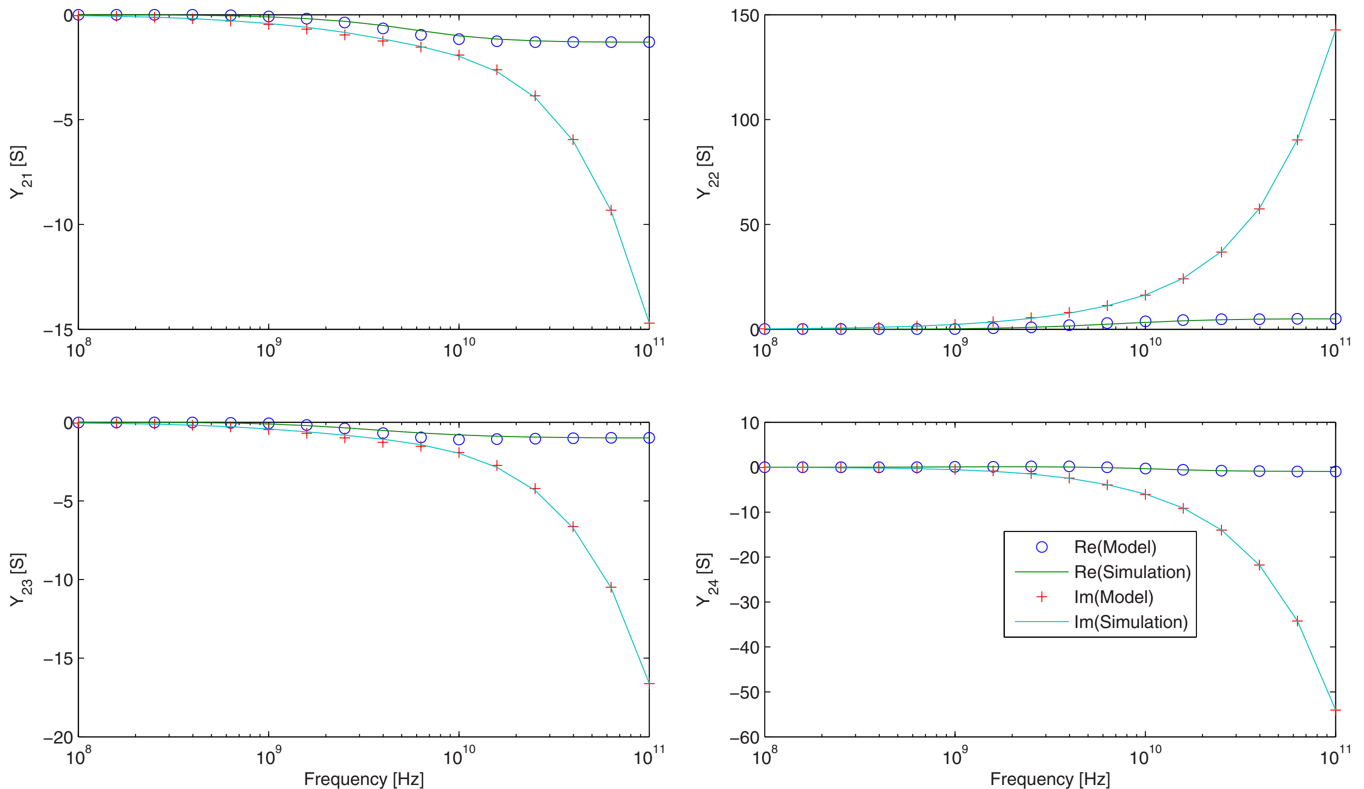


Fig. 4. Admittance parameters related to TSV 2 showing good agreement to simulation.

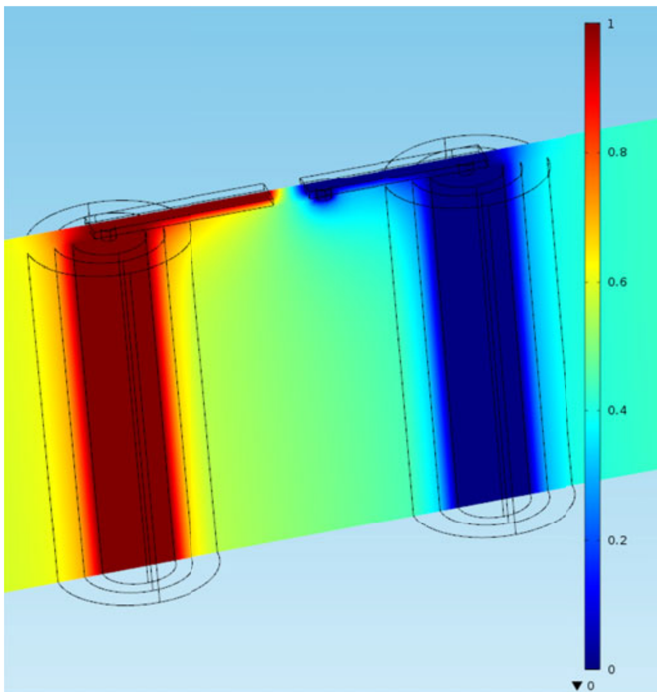


Fig. 5. Voltage distribution between a signal and ground TSV including redistribution layers and a substrate contact.

Hence, general RLC passivity enforcement techniques such as [26], which seek positive residues for all real poles, would fail to accurately generate an *RC* model.

A convenient method to fit the admittance of an *RC* network is through Y_{RC}/s rather than Y_{RC} as

$$\frac{Y_{RC}}{s} = a + \sum_{i=1}^{N} \frac{k_i}{s - p_i}. \tag{6}$$

Unlike Y_{RC}, the partial fraction expansion of Y_{RC}/s has a positive constant term as well as positive residues. The positive constraint can again be enforced using non-negative least squares.

A. Numerical Example

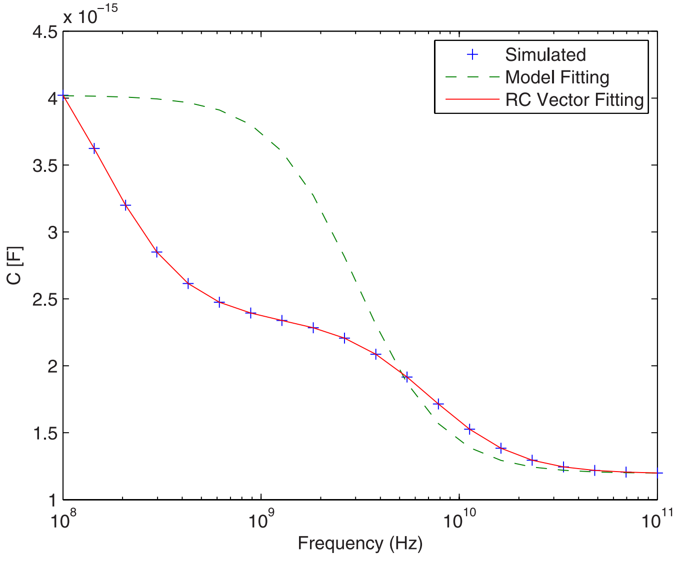
An example for the application of *RC* vector fitting is shown in Fig. 5, which was simulated using COMSOL 3-D electric current simulator. The properties of the substrate for this simulation are the same as in the example of Fig. 3, except that circular TSVs with a radius of 1μm and pitch of 10μm have been used. The substrate thickness is 10μm. Because of the 3-D field coupling between the TSVs, wires on redistribution layers, and substrate contact; the conductance and capacitance have complicated behaviors that cannot be fit into an *RC* model using the model topology in Fig. 1.

The results are shown in Fig. 6. There is an excellent agreement using *RC* vector fitting, as opposed to the model fitting attempt, which shows large discrepancy. The *RC* vector fitting used only three poles to fit Y_{RC} in (6). For this example, standard least squares provided already positive terms, so there was no need to use non-negative least squares.

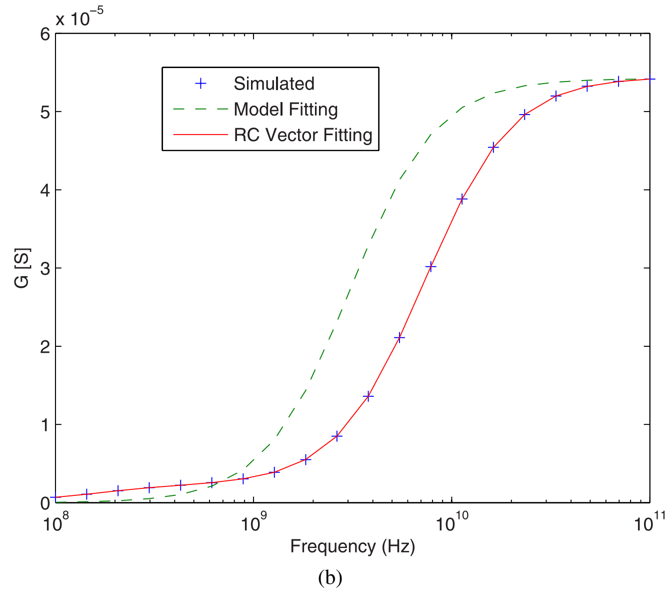
This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

TABLE I
COMPARISON OF STANDARD VECTOR FITTING ALGORITHM VERSUS PROPOSED *RC* VECTOR FITTING FOR GUARANTEED PASSIVE MACROMODELING OF 3-D IC INTERCONNECTS

Standard vector fitting	New RC vector fitting
The starting poles can be real or complex	Poles limited to stable real poles only
The residues can be positive or negative	Positive residues using non-negative least squares
(Possibly) non-passive RLC network	Passive RC network

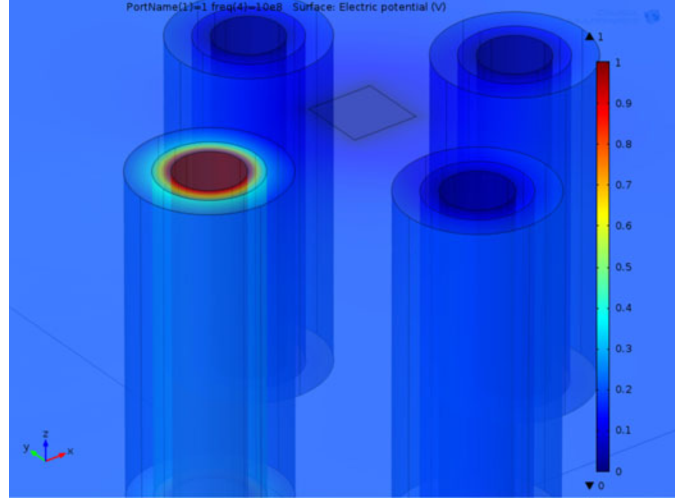


(a)

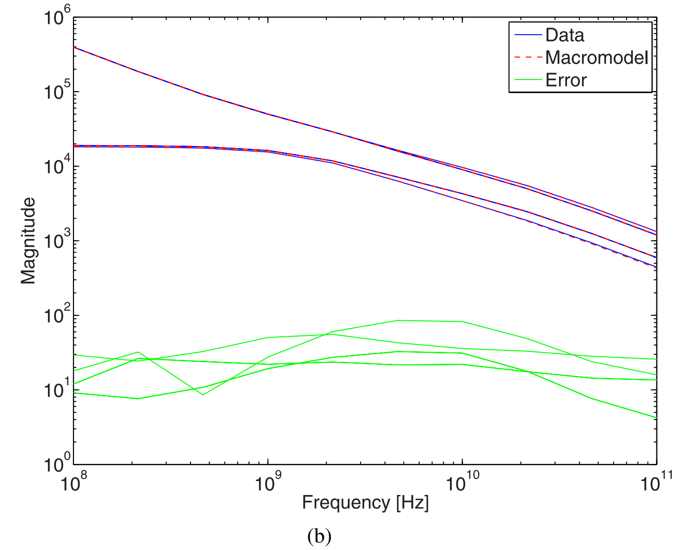


(b)

Fig. 6. (a) Capacitance and (b) conductance of the configuration in Fig. 5. Fitting to a prespecified topology (model fitting) is not accurate; whereas *RC* vector fitting using three poles provides excellent accuracy.



(a)



(b)

Fig. 7. (a) Three signal TSVs + 1 ground TSV with a substrate tap (ground) in the center of the array. (b) Good fit on all impedance parameters using standard vector fitting (no passivity enforcement) with three poles. (Note that, because of symmetry, there are only four independent impedance parameters: $Z_{11}, Z_{12}, Z_{22}, Z_{23}$, assuming that TSV 1 is across the ground TSV).

IV. MULTIPORT *RC* VECTOR FITTING

Multiport *RC* vector fitting can be done similar to the one-port case that was described. Poles of the admittance function of a multiport *RC* network are also real and negative similar to the one-port case [27]. However, the passivity condition needs to be enforced on residue matrices and not on scalar residues. As such, the residue matrices $\mathbf{a}$ and $\mathbf{k_i}$ in (5) should be positive-semidefinite matrices (i.e., all eigenvalues should be positive). Once stable and real poles have been identified using standard vector fitting approach, fitting the residues becomes a least-squares problem with semidefinite constraints. Optimization problems of this type are convex and can be solved using semidefinite programming. The SeDuMi algorithm under the interface of the cvx package [29] has been used in this paper. In the following examples, Z_{RC} form as given in (5) was applied.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

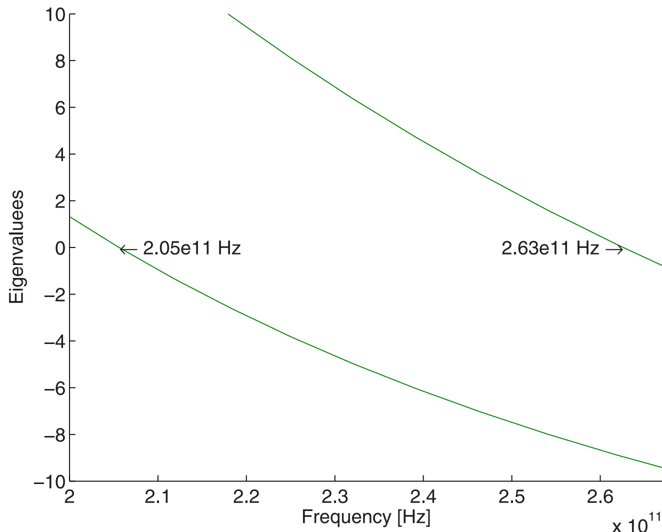


Fig. 8. Frequency sweep of all the eigenvalues of the real part of the impedance matrix. Passivity violation (i.e., negative eigenvalues) detected for the example in Fig. 7 at 2.06×10^{11} and 2.63×10^{11} Hz verifying the results of the passivity test method in [30].

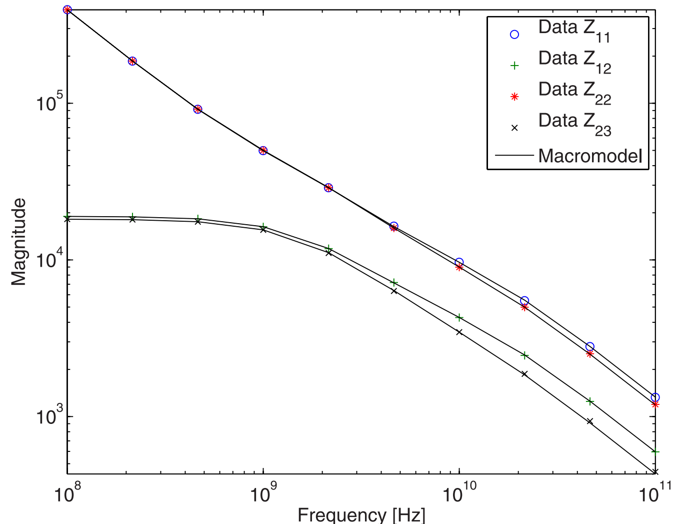


Fig. 9. Impedance matrix of the example in Fig. 7 based on the *RC* vector fitting approach resulting in an excellent fit while ensuring passivity using three poles.

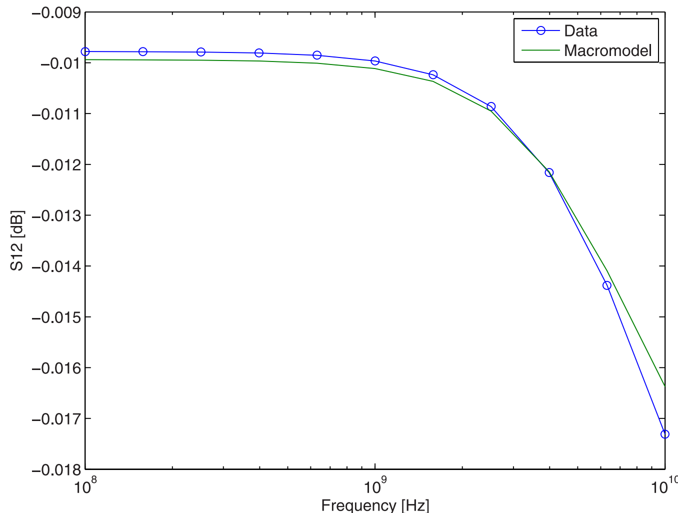


Fig. 10. *RC* vector fitting using three poles provides good fit to full-wave electromagnetic simulation using HFSS.

A. Numerical Examples

Consider the example shown in Fig. 7, which includes three signal TSVs and one ground TSV. The substrate is grounded with a square-shaped contact point in the center of the TSV array. First, a macromodel with three poles was created using the standard vector fitting algorithm. A good fit was achieved in all parameters as shown in Fig. 7.

The created model was observed to be nonpassive based on the passivity test in [30]. According to the test, passivity violation boundaries were calculated at 2.06×10^{11} and 2.63×10^{11} Hz. By sweeping the eigenvalues of the real part of the impedance matrix, the passivity violation was verified in this frequency range as shown in Fig. 8.

Next, a macromodel was generated by enforcing positive-definite residue matrices. The fitting is very good as shown in Fig. 9, and the network is guaranteed to be passive. The extracted rational function can be converted in a straightforward manner to an equivalent circuit model to do time-domain simulation of 3-D IC interconnects including nonlinear transistor models in SPICE. Since the generated model is passive, the macromodel does not cause instability in time-domain simulations.

To demonstrate the application of *RC* vector fitting on full-wave simulations, it is applied on a pair of TSVs that were considered in [18]. The 3-D full-wave simulator Ansys HFSS [31] is used on a similar configuration as in Fig. 7. In the HFSS simulation, only a signal and a ground TSV with a pitch of 10μm are considered, which resulted in a two-port model for the TSV pair. The *RC* vector fitting approach provides good fit on the insertion loss obtained from HFSS as shown in Fig. 10. To apply the *RC* vector fitting approach, the simulated S-parameters were converted to the impedance matrix. This caused discrepancy in fitting the data because an excellent fit was observed originally on the impedance matrix elements, even though the S-parameters in Fig. 10 indicate some discrepancy. In this example, three poles were used. The standard vector fitting algorithm once again resulted in a nonpassive model, which was corrected using the *RC* vector fitting approach.

V. Conclusion

This paper presented two methodologies to extract *RC* parasitic models for interconnects in a 3-D IC. The first methodology is model fitting of a prescribed equivalent circuit model to provided simulation data. This approach is suitable for TSVs of arbitrary cross section with predominantly 2-D field distribution.

The second methodology is *RC* vector fitting, where the circuit topology is also flexible. Based on this method, an *RC* model can be developed to fit 3-D electromagnetic simulations including the effects of substrate contacts, active circuits, and redistribution layers. For one-port networks, non-negative least

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

squares is used, whereas multiport macromodels can be generated using semidefinite programming. It has been shown that, even though standard algorithms may provide an excellent fit to simulated data, passivity violations may occur and can be corrected using the presented approach to generate an *RC* model without sacrificing accuracy.

REFERENCES

[1] S. Borkar, “Design challenges of technology scaling,” *IEEE Micro*, vol. 19, no. 4, pp. 23–29, Jul./Aug. 1999.

[2] M. Swaminathan and A. E. Engin, *Power Integrity Modeling and Design for Semiconductors and Systems*. Upper Saddle River, NJ, USA: Prentice Hall, 2007.

[3] Y. Zhang, X. Hu, A. Deutsch, A. Engin, J. Buckwalter, and C.-K. Cheng, “Prediction and comparison of high-performance on-chip global interconnection,” *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 19, no. 7, pp. 1154–1166, Jul. 2011.

[4] M. Motoyoshi, “Through-silicon via (TSV),” *Proc. IEEE*, vol. 97, no. 1, pp. 43–48, Jan. 2009.

[5] G. Hu, H. Kalyanam, S. Krishnamoorthy, and L. Polka, “Package technology to address the memory bandwidth challenge for tera-scale computing,” *Intel Technol. J.*, vol. 11, no. 3, pp. 197–206, Aug. 2007.

[6] J. Kim, J. S. Pak, J. Cho, E. Song, J. Cho, H. Kim, T. Song, J. Lee, H. Lee, K. Park, S. Yang, M.-S. Suh, K. yoo Byun, and J. Kim, “High-frequency scalable electrical model and analysis of a through silicon via (TSV),” *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 1, no. 2, pp. 181–195, Feb. 2011.

[7] J. S. Pak, J. Kim, J. Cho, K. Kim, T. Song, S. Ahn, J. Lee, H. Lee, K. Park, and J. Kim, “PDN impedance modeling and analysis of 3-D TSV IC by using proposed P/G TSV array model based on separated P/G TSV and chip-PDN models,” *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 1, no. 2, pp. 208–219, Feb. 2011.

[8] H. Kim, J. Cho, M. Kim, K. Kim, J. Lee, H. Lee, K. Park, K. Choi, H.-C. Bae, J. Kim, and J. Kim, “Measurement and analysis of a high-speed tsv channel,” *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 2, no. 10, pp. 1672–1685, Oct. 2012.

[9] J. R. Cubillo, R. Weerasekera, G. Katti, and R. Patti, “Through silicon interposer TSI co-design optimization for high performance systems,” in *Proc. Electron. Packag. Technol. Conf.*, Dec. 2012, pp. 93–98.

[10] I. Savidis and E. Friedman, “Closed-form expressions of 3-D via resistance, inductance, and capacitance,” *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 1873–1881, Sep. 2009.

[11] G. Katti, M. Stucchi, K. De Meyer, and W. Dehaene, “Electrical modeling and characterization of through silicon via for three-dimensional ICs,” *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 256–262, Jan. 2010.

[12] C. Xu, H. Li, R. Suaya, and K. Banerjee, “Compact AC modeling and performance analysis of through-silicon vias in 3-D ICs,” *IEEE Trans. Electron Devices*, vol. 57, no. 12, pp. 3405–3417, Dec. 2010.

[13] J. S. Pak, J. Cho, J. Kim, J. Lee, H. Lee, K. Park, and J. Kim, “Slow wave and dielectric quasi-TEM modes of metal-insulator-semiconductor (MIS) structure through silicon via (TSV) in signal propagation and power delivery in 3-D chip package,” in *Proc. 60th IEEE Electron. Compon. Technol. Conf.*, Jun. 2010, pp. 667–672.

[14] N. Khan, S. Alam, and S. Hassoun, “Mitigating TSV-induced substrate noise in 3-D ICs using GND plugs,” in *Proc. 12th Int. Symp. Quality Electron. Design*, Mar. 2011, pp. 1–6.

[15] C. Xu, R. Suaya, and K. Banerjee, “Compact modeling and analysis of through-Si-via-induced electrical noise coupling in three-dimensional ICs,” *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 4024–4034, Nov. 2011.

[16] D. H. Kim, S. Mukhopadhyay, and S. K. Lim, “Fast and accurate analytical modeling of through-silicon-via capacitive coupling,” *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 2, pp. 168–180, Feb..

[17] J. Zheng, Y.-C. Hahm, V. Tripathi, and A. Weisshaar, “CAD-oriented equivalent-circuit modeling of on-chip interconnects on lossy silicon substrate,” *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 9, pp. 1443–1451, Sep. 2000.

[18] A. Engin and S. Narasimhan, “Modeling of crosstalk in through silicon vias,” *IEEE Trans. Electromagn. Compat.*, vol. 55, no. 1, pp. 149–158, Feb. 2013.

[19] A. E. Engin, “Equivalent circuit model extraction for interconnects in 3-D ICs,” in *Proc. Asia South Pacif. Design Autom. Conf.*, 2013, pp. 1–6.

[20] Comsol version 4.2, [Online]. Available: http://www.comsol.com

[21] A. E. Engin, “Text Debye model fitting for time-domain modeling of lossy dielectrics,” in *Proc. IMAPS 43rd Int. Symp. Microelectron.*, Nov. 2010.

[22] B. Gustavsen and A. Semlyen, “Rational approximation of frequency domain responses by vector fitting,” *IEEE Trans. Power Del.*, vol. 14, no. 3, pp. 1052–1061, Jul. 1999.

[23] B. Gustavsen, “Fast passivity enforcement for S-parameter models by perturbation of residue matrix eigenvalues,” *IEEE Trans. Adv. Packag.*, vol. 33, no. 1, pp. 257–265, Feb. 2010.

[24] A. Lamecki and M. Mrozowski, “Equivalent spice circuits with guaranteed passivity from nonpassive models,” *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 3, pp. 526–532, Mar. 2007.

[25] S. Grivet-Talocia and A. Ubolli, “A comparative study of passivity enforcement schemes for linear lumped macromodels,” *IEEE Trans. Adv. Packag.*, vol. 31, no. 4, pp. 673–683, Nov. 2008.

[26] L. de Tommasi, D. Deschrijver, and T. Dhaene, “Single-input-single-output passive macromodeling via positive fractions vector fitting,” in *Proc. IEEE 12th Workshop Signal Propag. Interconn.*, May. 2008, pp. 1–2.

[27] K. Kerns and A. Yang, “Stable and efficient reduction of large, multiport RC networks by pole analysis via congruence transformations,” *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 16, no. 7, pp. 734–744, Jul. 1997.

[28] L. Weinberg. (1975). *Network analysis and synthesis*, ser. McGraw-Hill electrical and electronic series. R. E. Krieger Pub. Co., [Online]. Available: http://books.google.com/books?id=-etSAAAAMAAJ

[29] M. Grant and S. Boyd, “Graph implementations for nonsmooth convex programs,” in *Recent Advances in Learning and Control*, (Lecture Notes in Control and Information Sciences Series), V. Blondel, S. Boyd, and H. Kimura, Eds. New York, NY, USA: Springer-Verlag, 2008, pp. 95–110.

[30] A. Semlyen and B. Gustavsen, “A half-size singularity test matrix for fast and reliable passivity assessment of rational models,” *IEEE Trans. Power Del.*, vol. 24, no. 1, pp. 345–351, Jan. 2009.

[31] Ansys HFSS v13.0, [Online]. Available: http://www.ansys.com

A. Ege Engin (M’05) received the B.S. and M.S. degrees in electrical engineering from Middle East Technical University, Ankara, Turkey, and from University of Paderborn, Paderborn, Germany in 1998 and 2001, respectively, and the Ph.D. degree from the University of Hannover, Hannover, Germany, in 2004.

He was a Research Engineer at the Fraunhofer Institute for Reliability and Microintegration in Berlin, Germany. From 2006 to 2008, he was an Assistant Research Director of the Microsystems Packaging Research Center, Georgia Tech. He is currently an Associate Professor in the Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA, USA. He has more than 100 publications in journals and conferences in the areas of signal and power integrity modeling and simulation and four patents. He is the co-author of the book *Power Integrity Modeling and Design for Semiconductors and Systems*.

Dr. Engin received the Semiconductor Research Corporation Inventor Recognition Award in 2009. He has co-authored publications that received the Outstanding Poster Paper Award in the Electronic Components and Technology Conference 2006, the Best Paper of the Session Award from the International Microelectronics and Packaging Society in 2009, and was the Best Paper Award Finalist in the Board-Level Design Category, DesignCon 2007.