# Virtual Ground Fence for GHz Power Filtering on Printed Circuit Boards

A. Ege Engin, Member, IEEE, and Jesse Bowman

Abstract—In mixed-signal systems, noise coupling between different domains, such as digital and RF, can be a critical problem. Especially, the power/ground planes in packages or boards can be a major factor for noise coupling. Simultaneously switching drivers causes supply voltage fluctuations which can propagate both horizontally and vertically between the power/ground planes. The sensitive RF/analog signals have to be isolated from this digital switching noise, which gets coupled through the shared power distribution system. Hence, accurate estimation and improvement of the performance of power/ground planes is critical in a mixedsignal system. This paper introduces a new methodology to minimize the transfer impedance of the power distribution system. This will be achieved by a new design methodology, called the virtual ground fence. At its basic level, the virtual ground fence consists of quarter-wave transmission line stubs that act as short circuits between power and ground planes at their design frequency. An array of such stubs can then be considered as a ground fence. Power filtering is currently achieved mainly by using discrete decoupling capacitors at low frequencies. The virtual ground fence design is the distributed analog of this methodology at the gigahertz frequency regime.

Index Terms—Power and ground planes, power distribution network, power integrity, simultaneous switching noise.

#### I. INTRODUCTION

SHARED power supply is commonly used for digital and analog/RF components to reduce cost. However, noise coupling between different domains, such as digital and RF, can be a critical problem. Especially, the power/ground planes in packages or boards can be a major factor for noise coupling. Simultaneously switching drivers causes supply voltage fluctuations which can propagate both horizontally and vertically between the power/ground planes. The sensitive RF/analog signals have to be isolated from this digital switching noise, which gets coupled through the shared power distribution system. Hence, accurate estimation and improvement of the performance of power/ground planes is critical in a mixed-signal system.

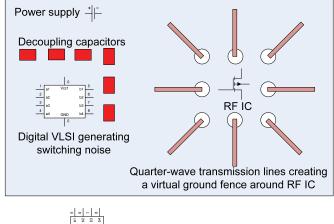
Manuscript received February 1, 2013; revised April 19, 2013; accepted May 16, 2013. Date of publication June 6, 2013; date of current version December 10, 2013.

A. E. Engin is with the Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA 92182 USA (e-mail: arifegeengin@gmail.com).

J. Bowman was with the Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA 92182 USA. He is now with Cubic Defense Applications, San Diego, CA 92123 USA (e-mail: jesse.bowman2@gmail.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TEMC.2013.2265054



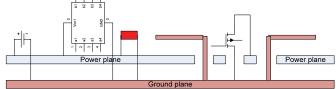


Fig. 1. Basic application of a VGF: Top view and side view.

The power supply noise generated by a digital very large scale integration (VLSI) can leak into other components, transmission lines, or power terminals of RF circuits. This noise mainly depends on the transfer impedance of the power distribution system between the IC generating the power supply noise and the sensitive components on a shared power distribution system. Hence, it is critical to minimize the transfer impedance of the power distribution system. For this purpose, we propose a new design methodology, called the virtual ground fence (VGF).

The basic idea of a VGF is shown in Fig. 1. There is switching noise generated by the digital VLSI. This noise easily propagates to the sensitive RF IC if not filtered. Filtering of highfrequency switching noise (in the gigahertz spectrum) is not possible using conventional techniques, such as decoupling capacitors and ferrite beads, because of the parasitic elements associated with discrete elements. Hence, there is a need for filtering high-frequency noise using distributed elements, where we propose to use VGF. At its basic level, the VGF consists of quarter-wave transmission line stubs that act as short circuits at their design frequency. An array of such stubs can then be considered as a ground fence. Hence, the power plane of the RF IC is effectively placed inside a Faraday cage, and isolated from the noise in the environment. Such transmission line stubs have been used before to enhance electromagnetic bandgap (EBG) structures [1], [2], but in our approach, a periodic EBG structure is not needed.

A good overview of conventional power filtering techniques is given in [3]. Shortcomings of existing techniques for power filtering can be summarized as follows.

- Decoupling capacitors and ferrite beads: With the increase
  in clock frequency of digital VLSI, the switching noise
  has considerable amount of energy at gigahertz spectrum.
  Even high-quality discrete components cannot be used to
  filter noise at gigahertz level, as the parasitic inductance
  and capacitance due to necessary pads and vias to mount
  the discrete components make them ineffective [4], [5].
- 2) Using thin laminates between the power and ground planes: This is the simplest technique that can be very effective for suppressing resonances and broadband power filtering [6]. Thin laminates, however, significantly increase the cost of the system. Also, ten times thinner laminate is required to reduce the transfer impedance magnitude by 20 dB, which may not be feasible if high isolation levels are required.
- 3) Power islands: This technique is based on using a moat around the isolated area which is connected to the power supply using a narrow bridge [7], [8]. At resonance frequencies of the power planes, there is substantial noise coupling through the conducting bridge. As such, power island methodology cannot be relied on to provide power filtering in the presence of power plane resonances.
- 4) EBG structures: These are periodic structures that are used as filters on a power plane (see, e.g., [9] and [10]). A major bottleneck in practical application of EBG structures is the lack of a design methodology for given bandgap specifications. Design equations exist in the literature only for a few EBG types [11]–[13]. It is also difficult to have completely periodic EBG structures due to the presence of signal or stitching vias, which may impact the bandgap of the EBG [14]. The slits on the power or ground planes are also a big concern for return currents when high-frequency transmission lines need to traverse over them [15]–[17] causing increased reflection, crosstalk, and radiation. The slits also increase the IR drop on the power plane.

The VGF overcomes all of these shortcomings as it is based on simple transmission line stubs that can be designed using microwave filter design theory. There are also no slits to interrupt current paths. With the increased frequencies of off-chip signals, we anticipate that the VGF technology will become as important as decoupling capacitors and ferrite beads that are used for isolation and decoupling at low frequencies. We introduced the concept of VGF for the first time in [18]–[20]. In this paper, we will present test board designs and characterizations to validate our results.

#### II. DECOUPLING STUBS

A VGF consists of transmission line stubs that are shorted to the power plane but routed on the ground plane, as shown in Fig. 2(a). The stubs are left unterminated. At the basic level, the stubs are quarter wavelength, hence convert the open circuit at the far end to a short circuit between the power and ground planes at the via location. Due to the presence of this ac short circuit

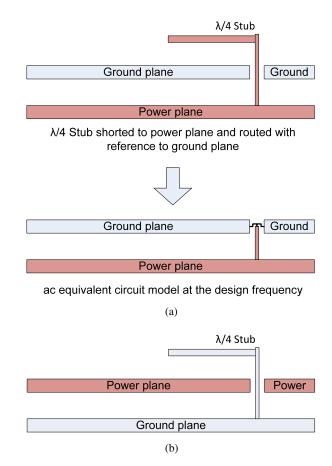


Fig. 2. (a) Quarter-wave stubs convert the open circuit at the far end to an ac short circuit between the power and ground planes at the via location. (b) Another possible configuration where ground stubs instead of power stubs are used.

cuit between the power and ground planes, effectively a ground fence can be created around a sensitive area of the power plane by using an array of such stubs. Another possible configuration is a ground stub that is routed on the power plane, as shown in Fig. 2(b).

The orientation of the stubs is not important and spiral resonators can decrease the total area needed for the stubs. The distance between the stubs should be electrically small at its design frequency. In the designed test boards, the distance was chosen to be less than  $\lambda/10$ . The stubs should completely surround the area to be isolated. They can also be distributed across the board, which may be useful to provide a whole-board isolation for all components that share the same power plane.

## III. VIRTUAL GROUND FENCE

To illustrate the effectiveness of the VGF, a test structure is simulated using the full-wave electromagnetic simulator Sonnet. A 3-D view of the layout is shown in Fig. 3(a). The stack-up consists of dielectrics with a thickness of 200 um, dielectric constant of 4, and loss tangent of 0.025. Two ports close to two opposite corners have been defined. To reduce the coupling between the two ports at around 2 GHz, a VGF consisting of three quarter-wave stubs has been used. Compared to the solid

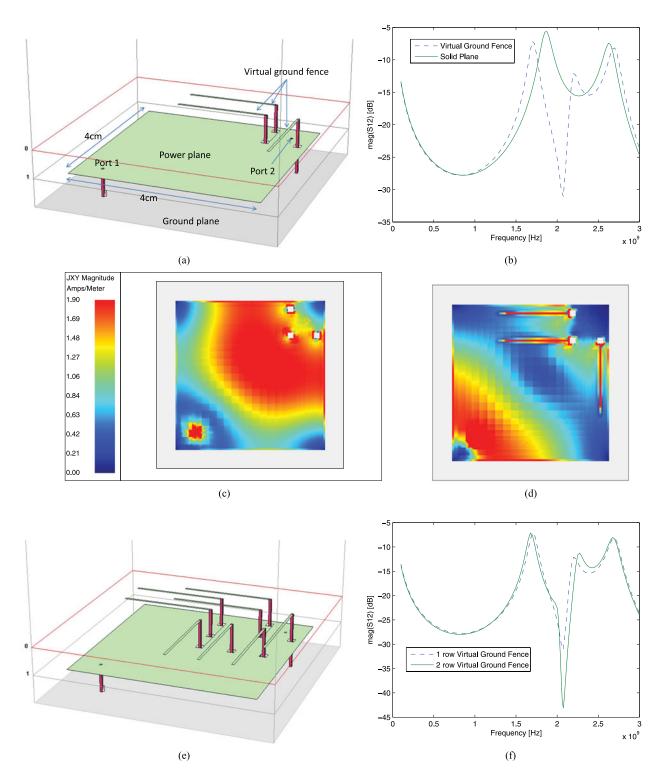


Fig. 3. (a) Geometry of the VGF. (b) Isolation increased by more than 20 dB by using VGF. (c) Current distribution of top plane with no stubs at 2.05 GHz. (d) Current distribution with VGF at 2.05 GHz. (e) Geometry of the two-row VGF. (f) Isolation increased by including a second row.

plane case, isolation could be increased by more than 20 dB using only a single row of three stubs, as shown in Fig. 3(b). The current distribution without the VGF is shown in Fig. 3(c). The excitation is a 1-V voltage source with  $50-\Omega$  impedance. It can be observed that with the addition of the VGF in Fig. 3(d), noise current is blocked and effectively a Faraday cage is created around the isolation area.

To increase the isolation level, additional rows can be included in the VGF. As an example, a two-row VGF is shown in Fig. 3(e) and compared with the previously discussed one-row case in Fig. 3(f). Substantial increase in isolation level can be seen.

Due to the use of quarter-wave stubs, the bandwidth of isolation narrows. Therefore, this method is most suitable for achieving isolation in narrow-band systems. As an application of this

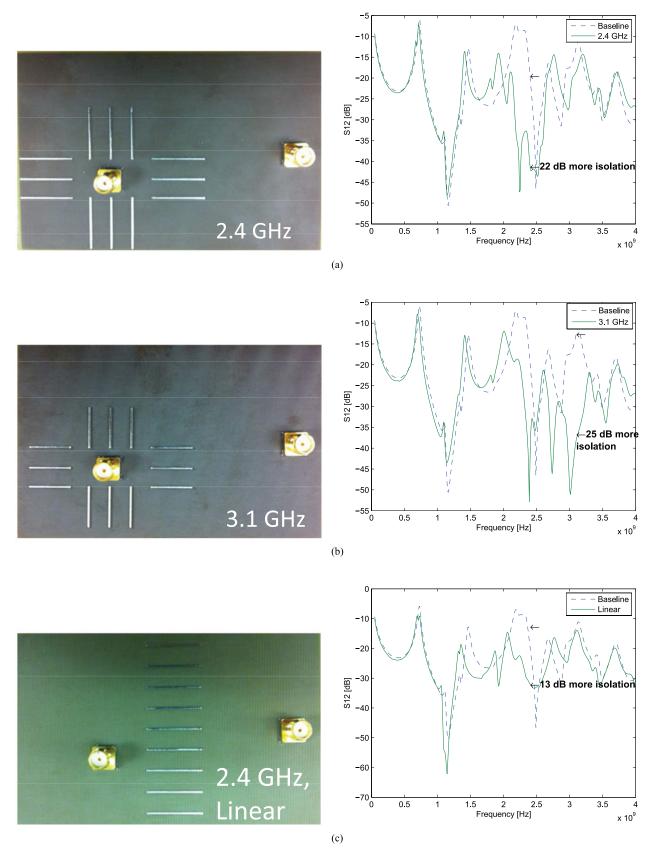
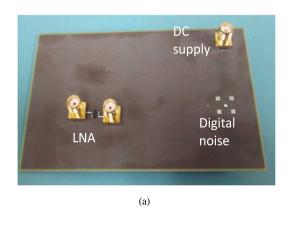
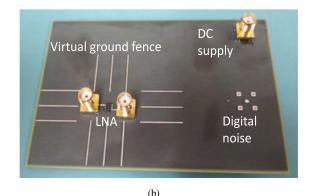


Fig. 4. (a) VGF designed at 2.4 GHz. (b) VGF designed at 3.1 GHz. (c) VGF designed at 2.4 GHz to provide half-board isolation. The baseline board design consists of solid power and ground planes.





No digital noise Baseline with digital noise Virtual Ground Fence with digital noise 20 16 Noise Figure [dB 10 1.75 1.85 1 95 2 05 2 25 2 35 2 45 2 65 2 75 Frequency [GHz] (c)

Fig. 5. Active test board to measure the noise figure of a 2.4-GHz LNA. (a) Baseline board. (b) VGF designed at 2.4 GHz. (c) VGF was able to block digital noise at its design frequency; hence, the noise figure was maintained in the presence of digital noise at around 2.4 GHz.

methodology, an RF chip can be protected at its operating frequency from a noisy digital chip. Even though the switching noise generated by the digital chip is broadband, the objective is reducing its effect on the narrow-band RF chip. For some applications, it may be desired to have wider isolation bandwidth. The characteristic impedance of the stubs do not necessarily have to be  $50\,\Omega$ . The input impedance of a quarter-wave stub can be calculated using the well-known formula  $Z_{\rm stub} = Z_0 \, {\rm coth}(\gamma l)$ , where  $\gamma$  is the propagation constant, l is the length, and  $Z_0$  is the characteristic impedance of the stub. Hence, the impedance of the stubs is linearly proportional to the characteristic impedance. Therefore, wider traces are preferable in increasing both the isolation level and bandwidth.

#### IV. PASSIVE TEST BOARDS

Several test boards containing VGF are designed and characterized for hardware verification of their isolation property. All test boards are of size  $3.8^{\prime\prime} \times 2.5^{\prime\prime}$  with four layers where the inner two layers are power and ground planes. The dielectric between power and ground planes is FR-4, having a thickness of 28 mils, and dielectric constant of 4.6. The planes are made of 1 oz copper. In total, a baseline test board and three VGF test boards were designed and characterized.

- 1) Baseline: Solid power and ground planes were used without the VGF.
- 2) 2.4 GHz: A small portion of the power plane was isolated by surrounding it with 12 ground stubs at 2.4 GHz.

- 3) 3.1 GHz: Same design was repeated but the stubs were designed to resonate at 3.1 GHz.
- 4) Linear: In the center of the board, a linear array of nine decoupling stubs were placed to achieve half-board isolation at 2.4 GHz.

The measurement of the test boards confirmed the isolation characteristics of the VGF as shown in Fig. 4, compared to the baseline board, which was not populated with stubs. In all test boards, the VGF has operated as expected and provided isolation at the design frequency. As an example, the measurements shown in Fig. 4(a) indicate that the VGF has achieved 22 dB more isolation than the baseline board at the design frequency of 2.4 GHz. The response is similar to the baseline board at other frequencies.

By reducing the length of the resonators, the isolation can simply be moved to a higher frequency. As an example, the 3.1-GHz test board uses shorter resonators and has achieved 25-dB isolation at the design frequency.

Half-board isolation can be achieved if the total board is divided by an array of decoupling stubs. The linear array of decoupling stubs has achieved 13-dB isolation at the design frequency of 2.4 GHz, which was less than the 22-dB isolation observed in the previous case. This indicates that the location of the resonators is an important parameter.

Addition of the stubs can, in general, lower the routing density of the board; however, these examples suggest that there is sufficient room to route multiple traces across the VGF. Such traces would not suffer from a return path discontinuity, as they are routed over a continuous plane.

### V. ACTIVE TEST BOARDS

An active test board was also designed to observe the impact of digital switching noise on the noise figure in the example of a low-noise amplifier (LNA). The LNA was placed in the center of the VGF to verify its isolation property. To introduce the digital noise into the active test board, a pseudorandom bit sequence at a clock frequency of 1.5 GHz with a full voltage swing of 100 mV was applied between the power and ground planes. The applied digital signal provided broadband excitation of power plane noise across the test frequencies of 1.7–2.8 GHz. The 2.4-GHz LNA was powered through a dc source of 3 V that was supplied to the board with an SMA connector. Next, the noise figure of the LNA was measured with and without a VGF. The noise figure was measured with and without digital noise applied on the board.

Fig. 5 shows the active test board setup. In the presence of digital noise, the noise figure of the LNA in baseline board increases dramatically as shown in Fig. 5(c). When the VGF is applied, an increase in noise figure is still observed. However, the VGF is designed at the intended operating frequency of the LNA, which is 2.4 GHz. It can be observed that the VGF was able to block digital noise at its design frequency; hence, the noise figure was maintained in the presence of digital noise at around 2.4 GHz.

# VI. CONCLUSION

This paper introduced the VGF. This new method can effectively filter high-frequency noise generated by digital circuits. A VGF consists of quarter-wave ground stubs routed on the power plane. Hence, at the design frequency, there is an ac short circuit between power and ground planes, blocking any field propagation between them.

The test boards demonstrated the substantial noise reduction that can be achieved if RF circuits operating at the design frequency are placed inside the VGF. The simple design of the VGF for different frequencies was demonstrated by changing the isolation frequency of a given design from 2.4 to 3.1 GHz by changing the length of the resonators. Different implementations of the VGF can be used to achieve half-board or small-area isolation. An active test board with a VGF demonstrated that the noise figure of an LNA was not affected in the presence of digital switching noise on the power and ground planes.

This new and simple concept can serve as a distributed circuit approach for power decoupling and filtering, providing a solution at the gigahertz frequency regime, where discrete decoupling capacitors do not work.

#### REFERENCES

- B. Kim and D.-W. Kim, "Improvement of simultaneous switching noise suppression of power plane using localized spiral-shaped EBG structure and lambda/4 open stubs," in *Proc. Asia-Pacific Microw. Conf.*, Dec. 2007, pp. 1–4.
- [2] Y. Kasahara, H. Toyao, and T. Harada, "Open stub electromagnetic bandgap structure for 2.4/5.2 GHz dual-band suppression of power plane noise," in *Proc. IEEE Electr. Des. Adv. Packag. Syst. Symp.*, Dec. 2011, pp. 1–4.
- [3] T.-L. Wu, H.-H. Chuang, and T.-K. Wang, "Overview of power integrity solutions on package and PCB: Decoupling and EBG isolation," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 2, pp. 346–356, May 2010.
- [4] M. Swaminathan and A. E. Engin, Power Integrity Modeling and Design for Semiconductors and Systems. Upper Saddle River, NJ, USA: Prentice-Hall, 2007.
- [5] S. Weir, "PDN application of ferrite beads," in *Proc. Design Conf.*, Feb. 2011, pp. 1–4.
- [6] D. Iguchi and H. Umekawa, "A signal and power integrity oriented packaging for low cost and high performance systems," in *Proc. IEEE CPMT Symp, Japan*, Dec. 2012, pp. 1–4.
- [7] W. Cui, J. Fan, H. Shi, and J. Drewniak, "Dc power bus noise isolation with power islands," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, 2001, vol. 2, pp. 899–903.
- [8] A. Engin, "Efficient sensitivity calculations for optimization of power delivery network impedance," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 2, pp. 332–339, May 2010.
- [9] M.-S. Zhang, Y.-S. Li, C. Jia, and L.-P. Li, "Simultaneous switching noise suppression in printed circuit boards using a compact 3-D cascaded electromagnetic-bandgap structure," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 10, pp. 2200–2207, Oct. 2007.
- [10] Y. Toyota, A. E. Engin, T. H. Kim, M. Swaminathan, and K. Uriu, "Stop-band prediction with dispersion diagram for electromagnetic bandgap structures in printed circuit boards," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Portland, OR, USA, Aug. 2006, pp. 807–811.
- [11] K. H. Kim and J. Schutt-Aine, "Design of EBG power distribution networks with VHF-band cutoff frequency and small unit cell size for mixed-signal systems," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 7, pp. 489–491, Jul. 2007.
- [12] T.-K. Wang, C.-Y. Hsieh, H.-H. Chuang, and T.-L. Wu, "Design and modeling of a stopband-enhanced EBG structure using ground surface perturbation lattice for power/ground noise suppression," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 8, pp. 2047–2054, Aug. 2009.

- [13] B. Mohajer-Iravani and O. Ramahi, "Wideband circuit model for planar EBG structures," *IEEE Trans. Adv. Packag.*, vol. 33, no. 1, pp. 169–179, Feb. 2010.
- [14] F. de Paulis, L. Raimondo, and A. Orlandi, "Impact of shorting vias placement on embedded planar electromagnetic bandgap structures within multilayer printed circuit boards," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 7, pp. 1867–1876, Jul. 2010.
- [15] S.-G. Kim, H. Kim, H. do Kang, and J.-G. Yook, "Signal integrity enhanced EBG structure with a ground reinforced trace," *IEEE Trans. Electron. Packag. Manuf.*, vol. 33, no. 4, pp. 284–288, Oct. 2010.
- [16] F. De Paulis and A. Orlandi, "Signal integrity analysis of single-ended and differential striplines in presence of EBG planar structures," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 9, pp. 554–556, Sep. 2009.
- [17] A. Scogna, A. Orlandi, and V. Ricchiuti, "Signal and power integrity analysis of differential lines in multilayer printed circuit boards with embedded electromagnetic bandgap structures," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 2, pp. 357–364, May 2010.
- [18] A. Engin and J. Bowman, "Virtual ground fence: A methodology for GHz power filtering on printed circuit boards," in *Proc. Asia-Pacif. Symp. Electromagn. Compat.*, May 2012, pp. 421–424.
- [19] J. Bowman and A. E. Engin, "Virtual ground fence for power filtering on IC packages and printed circuit boards," in *Proc. IMAPS Adv. Technol.* Workshop Tabletop Exhib. RF Microw. Packag., Feb. 2012.
- [20] J. Bowman and A. E. Engin, "Virtual ground fence: A simple method for protection against high frequency simultaneous switching noise," in *Proc. IMAPS 45th Int. Symp. Microelectron.*, Sep. 2012.



Jesse Bowman was born in San Diego, CA, USA, in 1981. He received the Bachelor of Science degree in electrical engineering from San Diego State University, San Diego, in the fall of 2009. He continued his education with San Diego State University and completed the Masters of Science degree with an emphasis in electromagnetic systems in spring 2013.

He is currently working for Cubic Defense Applications, San Diego, as an RF Engineer.



A. Ege Engin (M'05) received the B.S. degree from Middle East Technical University, Ankara, Turkey, and the M.S. degree from University of Paderborn, Paderborn, Germany, in 1998 and 2001, respectively, both in electrical engineering. He received the Ph.D. degree (Summa Cum Laude) from the University of Hannover, Hannover, Germany in 2004.

He worked as a Research Engineer at the Fraunhofer-Institute for Reliability and Microintegration in Berlin, Germany. From 2006 to 2008, he was an Assistant Research Director of the Microsys-

tems Packaging Research Center at Georgia Tech. He is currently an Assistant Professor in the Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA, USA. He has more than 100 publications in journals and conferences in the areas of signal and power integrity modeling and four patents. He is the coauthor of the book *Power Integrity Modeling and Design for Semiconductors and Systems* (New York, NY, USA: Prentice-Hall, 2007).

Dr. Engin is the recipient of the Semiconductor Research Corporation Inventor Recognition Award in 2009. He has co-authored publications that received the Outstanding Poster Paper Award in the Electronic Components and Technology Conference 2006, the Best Paper Award Finalist in the Board-Level Design Category at DesignCon 2007, and the Best Paper of the Session Award in IMAPS Advanced Technology Workshop on RF and Microwave Packaging 2009