ARIF EGE ENGIN

Curriculum Vitae

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Education

2001–2004 **PhD (Summa Cum Laude) in Electrical and Electronics Engineering**, *University of Hannover*, Germany.

Modeling of Lossy Interconnects and Packages with Non-Ideal Power/Ground Planes

- 1998–2001 **MS in Electrical and Electronics Engineering**, *University of Paderborn*, Germany. Dyadic Green's Function for Stratified Media Using Complex Images
- 1993–1998 BS in Electrical and Electronics Engineering, Middle East Technical University, Turkey.

Employment

- 2023-present **Chair**, *Department of Electrical & Computer Engineering*, San Diego State University (SDSU), San Diego CA.
- 2019-present **Professor**, SDSU.
 - 2013–2019 Associate Professor, SDSU.
 - 2008–2013 Assistant Professor, SDSU.
 - 2005–2008 Assistant Research Director, Packaging Research Center, Georgia Institute of Technology, Atlanta GA.
 - 2001–2004 Research Engineer, Fraunhofer Institute for Reliability and Microintegration, Berlin, Germany.
 - 1999–2001 **Research Assistant**, Siemens C-Lab, Fraunhofer Institute for Reliability and Microintegration, Paderborn, Germany.

Awards

- 2017 IEEE EMC Society, Motohisa Kanda Award for the most cited paper in the last 5 years (2013-2017).
- 2016 International Symposium on Microelectronics, Best Paper of the Session Award, Pasadena, CA.
- 2015 Humboldt Foundation, Research Fellowship, Berlin, Germany.
- 2015 International Microelectronics Packaging and Assembly Society, Outstanding Educator Award.
- 2009 Advanced Technology Workshop on RF and Microwave Packaging, Best Paper of the Session Award, San Diego, CA.
- 2009 Semiconductor Research Corporation, GRC/FCRP/NRI Inventor Recognition Award.
- 2007 International Symposium on Microelectronics, Best Paper of the Session Award, San Jose, CA.
- 2007 DesignCon, Best Paper Award Finalist in Board-Level Design Category, Santa Clara, CA.
- 2006 ECTC, Outstanding Poster Paper Award, San Diego, CA.
- 2005 **Packaging Research Center**, *Award for the fastest start and program management*, Georgia Institute of Technology, Atlanta, GA.
- 2004 University of Hannover, Summa Cum Laude, Hannover, Germany.

2001 University of Paderborn, Dean's Award, Paderborn Germany.

Grants

- 2014–2019 NSF, Determination of High-Frequency Properties of Integrated Circuit Packages, \$291K, PI.
- 2016–2017 Sumitomo, Japan, Stepped Impedance Common-Mode Filter in Differential Lines, \$25K, PI.
- 2015–2018 Alexander-von-Humboldt Research Fellowship, Gigahertz Power Distribution Network Design, \$69K, Pl.
- 2013-2015 **Oak Mitsui Corporation**, Improved Signal Integrity Using Thin Dielectrics between Power and Ground Planes, Gift of \$15K, Pl.
- 2011–2013 **NEC Corporation, Japan**, *Efficient Simulation Methodology for Complex Power Delivery Networks*, \$80K, PI.
 - 2014 **Kyocera America**, *Dielectric Constant and Loss Tangent Characterization of Ceramic Packaging*, Gift of \$1K, Pl.
- 2011–2013 U.S. Air Force Research Laboratory, *Summer Visiting Faculty*, Electrical Design for Very-Large Scale 3D Integrated Systems, \$71K, PI.
- 2013–2014 **California Energy Commission**, *Electroporation of Algal Biomass to Enhance Methane Gas Production*, Co-PI.
- 2005–2007 **Panasonic**, *Panswitch-Customized Simultaneous Switching Noise Simulator*, \$250K, Co-PI at Georgia Institute of Technology.

Books and Patents

- 2007 **Power Integrity Modeling and Design for Semiconductors and Systems**, *Madhavan Swaminathan and A. Ege Engin*, Prentice Hall, November, 2007, ISBN: 0-13-615206-6, Translated to Japanese and Chinese.
- 2008 Chapter 4: Mixed Signal Design, in Introduction to System-on-Package (SOP), Madhavan Swaminathan, A. Ege Engin, Vinu Govind, Sidharth Dalmia, and Amit Bavisi, McGraw-Hill, March 2008, ISBN: 0071459065.
- 2021 A. E. Engin, G. Aguirre, K.-D. Lang, and I. Ndip. Non-overlapping power/ground planes for localized power distribution network design **United States Patent: US 2021/0153341 A1**. applications also filed in germany, china, and japan, May 2021.
- 2011 Tae Hong Kim, A. Ege Engin, and Madhavan Swaminathan. Systems and methods for electromagnetic band gap structure synthesis **United States Patent: 8,060,457**, November 2011.
- 2011 Arif Ege Engin and Madhavan Swaminathan. Multilayer finite difference methods for electrical modeling of packages and printed circuit boards **United States Patent: 7,895,540**, February 2011.
- 2010 Madhavan Swaminathan, A. Ege Engin, Prathap Muthana, and Krishna Srinivasan. Device having an array of embedded capacitors for power delivery and decoupling of high speed input/output circuitry of an integrated circuit **United States Patent: 7,705,423**, april 2010.
- 2009 Madhavan Swaminathan, A. Ege Engin, Prathap Muthana, and Lixi Wan. Packaging having an array of embedded capacitors for power delivery and decoupling in the mid-frequency range and methods of forming thereof **United States Patent: 7,504,706**, march 2009.



- F. Coronado and A. E. Engin, "Passos: Passive approximation through sum-of-squares orthogonal rational functions," *IEEE Transactions on Electromagnetic Compatibility*, vol. 65, no. 2, pp. 555–563, 2023.
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- [5] R. B. Paul, A. E. Engin, and J. Aguirre, "Dielectric and underfill characterization using cavity resonators for millimeter-wave applications," *IEEE Letters on Electromagnetic Compatibility Practice* and Applications, pp. 1–1, 2020.
- [6] W. A. Alarcon, A. E. Engin, I. Ndip, and K. Lang, "Ebg common-mode filter design using uncoupled coplanar waveguide to microstrip transitions," *IEEE Letters on Electromagnetic Compatibility Practice* and Applications, pp. 1–1, 2020.
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- [11] —, "Power plane filter using higher order virtual ground fence," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 7, no. 4, pp. 519–525, April 2017.
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Refereed Conferences

- A. Lemus and A. E. Engin, "Causal or not? a definite answer for frequency-response data," in 2023 IEEE 32nd Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), 2023, pp. 1–3.
- [2] A. Lemus, J. Settle, C. Akerlundh, and A. E. Engin, "Adaptive frequency sampling algorithm on a vna," in *IMAPS*, Oct 2023.
- [3] A. Lemus, F. Coronado, and A. E. Engin, "Adaptive generation of passive rational function approximations for electromagnetic simulation," in 2023 International Applied Computational Electromagnetics Society Symposium (ACES), 2023, pp. 1–2.
- [4] A. Lemus and A. E. Engin, "Adaptive generation of rational function approximations for microwave network parameters," in 2023 IEEE/MTT-S International Microwave Symposium - IMS 2023, 2023, pp. 235–238.
- [5] F. Coronado and A. E. Engin, "Passive modeling of interconnects using sum of squares partial fraction expansions," in 2022 IEEE Electrical Design of Advanced Packaging and Systems (EDAPS), 2022, pp. 1–3.
- [6] —, "Sum of squares partial fractions: Application in modeling of interconnects in heterogeneous integration," in *2022 IEEE ICSJ*, 2022, pp. 1–3.
- [7] —, "Passive modeling of one-port networks through sos orthogonal rational functions," in 2022 IEEE 26th Workshop on Signal and Power Integrity (SPI), 2022, pp. 1–4.
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- [11] A. E. Engin, I. Ndip, K. D. Lang, and J. Aguirre, "Differential-line characterization using mixed-port scattering parameters," in *IEEE NEMO*, Aug 2018.
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- [14] A. E. Engin, I. Ndip, K. D. Lang, and J. Aguirre, "Non-overlapping power/ground planes for localized power distribution network design," in 2016 IEEE Electrical Design of Advanced Packaging and Systems (EDAPS), Dec 2016, pp. 7–9.
- [15] A. E. Engin, I. Ndip, K. D. Lang, and G. Aguirre, "Determination of dielectric thickness, constant, and loss tangent from cavity resonators," in *IEEE EPTC*, Nov 2016.
- [16] A. E. Engin, I. Ndip, and K. D. Lang, "Higher-order virtual ground fence design for filtering power plane noise," in 2016 IEEE 20th Workshop on Signal and Power Integrity (SPI), May 2016, pp. 1–3.
- [17] A. E. Engin, "Stepped-impedance common-mode filter in differential lines," in 2016 IEEE CPMT Symposium Japan (ICSJ), Nov 2016, pp. 209–212.
- [18] Q. S. Su, A. E. Engin, and J. Aguirre, "Electrical characterization of low-profile copper foil for reduced surface roughness loss," in *IMAPS*, oct. 2016.
- [19] C. Ferguson and A. Engin, "Power archipelago for ghz power filtering on printed circuit boards," in *Electromagnetic Compatibility and Signal Integrity, 2015 IEEE Symposium on*, March 2015, pp. 193–196.
- [20] A. Ege Engin and J. Bowman, "Virtual ground fence options for shielding power plane noise," in *Electromagnetic Compatibility (EMC), 2014 IEEE International Symposium on*, Aug 2014, pp. 460–464.
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- [22] H. Dsilva and A. E. Engin, "Dielectric constant, loss tangent, and surface-roughness loss characterization of ceramic substrates," in IMAPS/ACerS International Conference and Exhibition on Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT),, apr. 2014.
- [23] A. Engin, "Equivalent circuit model extraction for interconnects in 3d ics," in *Design Automation Conference (ASP-DAC)*, 2013 18th Asia and South Pacific, 2013, pp. 1–6.
- [24] A. Engin, B. Adepu, M. Kusumoto, and T. Harada, "Macromodeling of complex power delivery networks for efficient transient simulation," in *CPMT Symposium Japan, 2012 2nd IEEE*, 2012, pp. 1–4.
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- [26] S. Raghavan N. and A. E. Engin, "High frequency signal propagation in through silicon vias," in IMAPS 45th International Symposium on Microelectronics, sep. 2012.

- [27] J. Bowman and A. E. Engin, "Virtual ground fence: A simple method for protection against high frequency simultaneous switching noise," in *IMAPS 45th International Symposium on Microelectronics*, sep. 2012.
- [28] A. Engin and N. Raghavan, "Modeling of coupled tsvs in 3d ics," in *Electromagnetic Compatibility* (EMC), 2012 IEEE International Symposium on, aug. 2012, pp. 7 –11.
- [29] J. Bowman and A. E. Engin, "Virtual ground fence for power filtering on ic packages and printed circuit boards," in IMAPS Advanced Technology Workshop and Tabletop Exhibition on RF and Microwave Packaging, feb 2012.
- [30] A. E. Engin and S. Raghavan N., "Metal semiconductor (MES) TSVs in 3D ICs: Electrical modeling and design," in IEEE International 3D System Integration Conference (3DIC), Feb. 2012.
- [31] A. Engin and J. Bowman, "Virtual ground fence: A methodology for ghz power filtering on printed circuit boards," in *Electromagnetic Compatibility (APEMC), 2012 Asia-Pacific Symposium on*, may 2012, pp. 421 –424.
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Service

SDSU

- 2022–2023 Faculty Search Committee Chair for Optics/Photonics.
- 2014–2020 Senator at the University Senate.
- 2008–present **Committee member**, Service at committees including the Department Reappointment Tenure and Promotion, College Constitution and Bylaws, Department/College Faculty Search, University Library, University Committee on Committees, Department/College/University Curriculum Committees.

Short courses

2024 Webinar instructor, *IEEE EPS Japan Meeting*, Electrical Modeling and Characterization for Heterogeneous Integration.

- 2023 **Professional development course instructor**, *IMAPS International Symposium*, Introduction to Power Integrity in Microelectronics Packaging.
- 2017 Lead speaker, *IMAPS San Diego Chapters Technical Presentation and Lunch*, High-Frequency Characterization of Chip Package Substrates.
- 2015 Clayton R. Paul Global EMC And SI University Instructor, *IEEE Symposium on Electromagnetic Compatibility and Signal Integrity*, Introduction to Power Integrity.
- 2012–2014 **Session Chair and Organizer**, *IEEE International Symposium on Electromagnetic Compatibility*, Fundamentals of Signal Integrity.
 - 2012 Lead speaker, IEEE Santa Clara Valley Electromagnetic Compatibility Mini Symposium (IEEE SCV-EMC 2012), 3/4 day speech on "Fundamentals of Signal and Power Integrity".
 - 2011 Keynote speaker, Signal Integrity & Power Integrity Technical Seminar, Electromagnetic Simulation for Power Integrity: From Analysis to Design.
 - 2011 Webinar instructor, Webinar to support Japan earthquake and tsunami relief, Electromagnetic Simulation for Power Integrity: From Analysis to Design.
- 2009–2010 **IMAPS webinar**, Electrical Modeling, Analysis and Optimization of Electronic Packaging Structures for Signal and Power Integrity.

Professional

- 2022–present Associate Editor, IEEE Transactions on EMC.
- 2019–2023 Board Member, IMAPS San Diego Chapter.
- 2021-present Editorial Board Member, Frontiers in Micro- and Nanoelectromechanical Systems.
- 2016–present **Paper Review Committee Member**, *IEEE Electrical Performance of Electronic Packaging Conference*.
 - 2015 NSF Panel Reviewer, Communications, Circuits, and Sensing-Systems (CCSS) program.
 - 2014 Student Activities Chair, International Symposium on Microelectronics, IMAPS.
- 2009–present Technical Program Committee Member, Electronics Packaging Technology Conference.
 - 2008 **Technical Program Committee Member**, *Electrical Design of Advanced Packaging & Systems Symposium*.